SOLID STATE FREQUENCY DOUBLERS

A Thesis submitted

In partial fulfilment of the requirements

For the Degree of

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by

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CERTIFICATE

Certified that this work on "Solid State Frequency Doublers" by Mr. A K Agrol has been carried out under my supervision and that this has not been submitted elsewhere for a degree.

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ABSTRACT

The development of a number of frequency doubler circuits has been discussed As the frequency doubler circuits with two phase input using two full wave rectifiers and a subtraction unit suffered from the drawbacks of low efficiency and poor regulation, an attempt was made to improve the circuits. This resulted in the development of an improved frequency doubler circuit with two phase input. The principles employed in the above circuits have been shown to be quite general for frequency multiplication Since a two phase input is necessary for these frequency doublers, an attempt was made to develop a frequency doubler with single phase input. This circuit also has been shown to be applicable for frequency multiplication by an integer greater than two

CHAPTER - I

INTRODUCTION

The development of Silicon Controlled Rectifier (SCR), a semiconductor equivalent of thyratron and mercury arc rectifier has given the electrical engineer a new tool for power control. Many interesting and valuable applications have been devised, the frequency changer being one of them.

A frequency changer is a device or a combination of devices that receives electrical power at a given frequency and delivers it at a different frequency. The voltage and number of phases may or may not be changed during the transformation process. However, this can be obtained by using static transformers. Hithertoo, the frequency conversion has been possible only by rotating machinery, inverter circuits or by frequency changers using ignitron, thyratron and saturable core reactors. The advantages of the static devices over the rotating machinery need no mention. But in the static devices also, the SCR has an edge over the other devices due to its high efficiency, low forward voltage drop and its firing instant being independent of both supply voltage and loading conditions.

The present work discusses the frequency doubler circuits using semiconductor devices, the rectifiers and thyristors (SCRs). The field of application of these circuits is in the flourescent lamps for lighting, high frequency welding and power supplies for high speed motors.

It is beyond the province of the present report to cover completely the characteristics of SCR, since the operation of frequency doublers discussed cannot be understood without the knowledge of these, the essentials are given.

(i) The SCR being a gate controlled rectifier differs considerably in operation from an ordinary rectifier. A semiconductor diode conducts when the threshold value of voltage is exceeded in the forward direction, but the controlled rectifier should have a positive gate to cathode voltage even when its anode is positive with respect to cathode.

(ii) Thyristor like the ordinary rectifier allows large currents to flow (depending upon its rating) with nearly constant but low voltage drop across it, when switched "on" (conducting) and a very small current through it when "off" (blocking).

(iii) The gating signal controls the triggering instant of SCR but when the current has started, the gate loses control.

(iv) SCR may be turned off either by allowing the anode voltage to go negative or interrupting the SCR current for a time exceeding the turn off time of the thyristor. The gate regains control when SCR stops conducting.

The thyristor thus is inherently a rectifier conducting only in one direction, whose conducting instant can be controlled.

The following chapters describe different circuits developed for frequency doubling. These circuits do not have an intermediate DC stage as in rectifier-inverter circuits.

Chapter II discusses a very simple circuit requiring a two phase A.C. supply input and gives out a single phase double frequency output. This circuit employs two full wave rectifiers and a subtraction unit. Though the output waveform is reasonably sinusoidal, its efficiency has been found to be very low.

Chapter III describes an improved frequency doubler circuit, where the subtraction of the two

rectifier A.C. inputs is made through the load. It is found that this circuit is more general and can be used for frequency multiplication by an integer using a proper balanced polyphase supply. The output waveform of this circuit is more distorted than that of the circuit explained in Chapter II. However it operates at a reasonably high efficiency.

In Chapter IV the conventional DC to AC inverter has been modified for use with single phase A.C. input. By properly chosing the gate circuit voltage, the circuit delivers power at twice the input frequency. The chief merit of this circuit is that it requires only single phase input. By using three such identical units, a three phase output at double the frequency can be obtained.

CHAPTER - II

FREQUENCY DOUBLERS WITH TWO PHASE INPUT

2.1 Introduction :

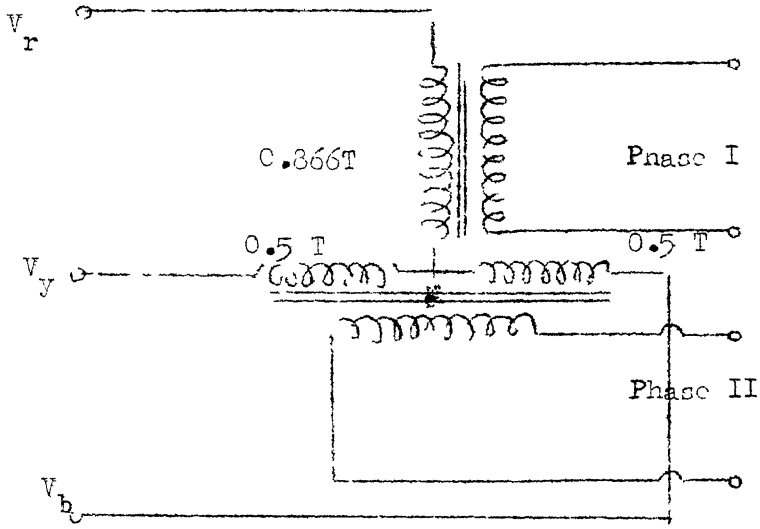
The frequency doubler circuits to be discussed use either diodes or both SCRs and diodes. The principle involved can be applied for frequency multiplication by a factor other than two also. The frequency multiplication factor being equal to the number of phases of the available supply Thus for frequency doubling two phase supply is needed This is obtained from three phase supply either by Scott connection (Fig.2.1a) or by directly making use of the phase relationship between the line voltage and a suitable phase voltage of the three phase supply (Fig.2.1b).

2.2 Principle :

The block diagram (Fig. 2.2) illustrates the principle involved. The two full wave rectifier units rectify the incoming sinusoidal signals and these signals are subtracted in the subtraction unit to give a double frequency output. The subtraction of the two rectified signals may be done either magnetically or electrically.

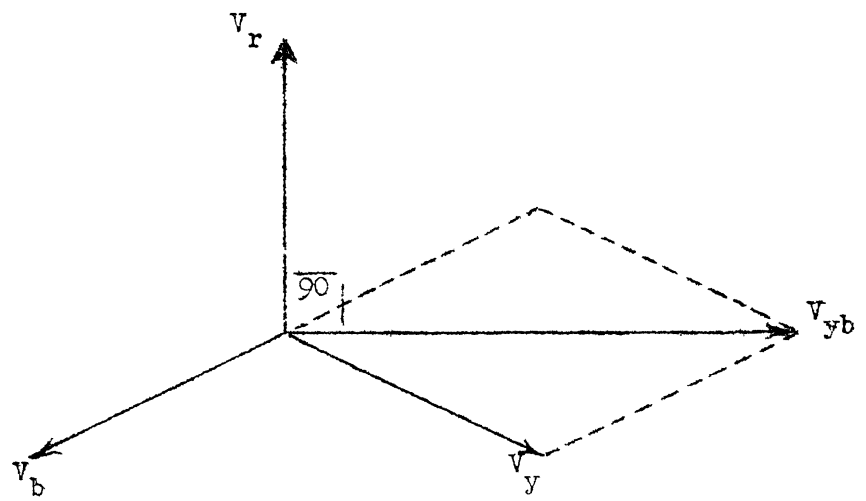
2.3 Circuits :

A few variations of the fundamental circuit as outlined in the Fig.2.2 will be discussed. The variations



Phase I and Phase II voltages are 90 degrees out of phase

Fig. 2.1 a Scott Connection



A phase voltage and a suitable line voltage are 90 degrees out of phase

Fig. 2.1 b

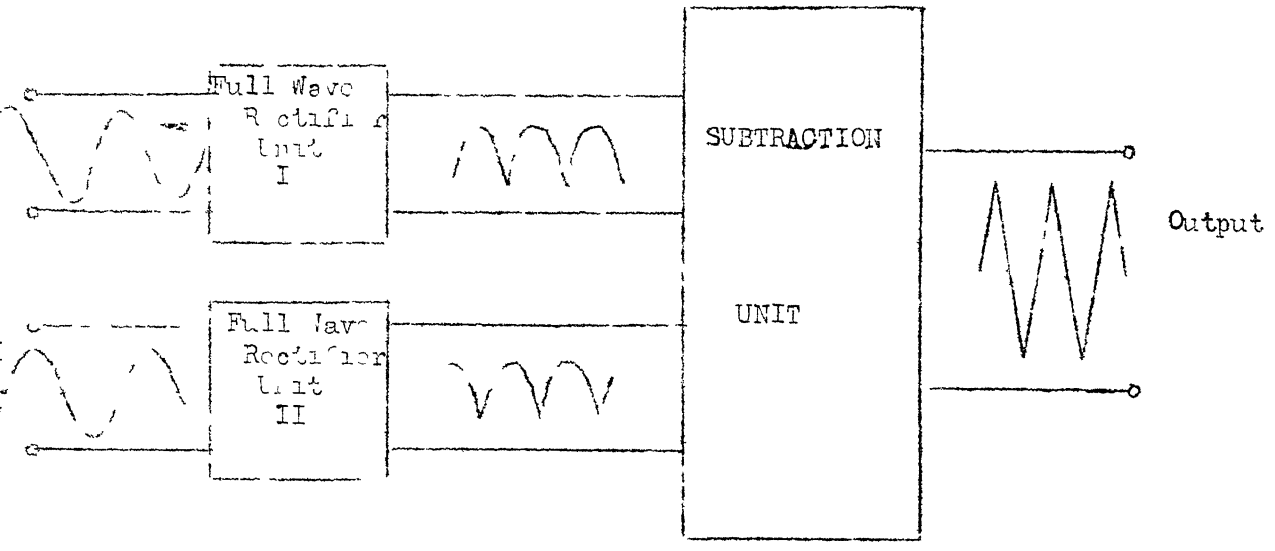


Fig.2.2

Block Diagram of a Frequency Doubler Circuit

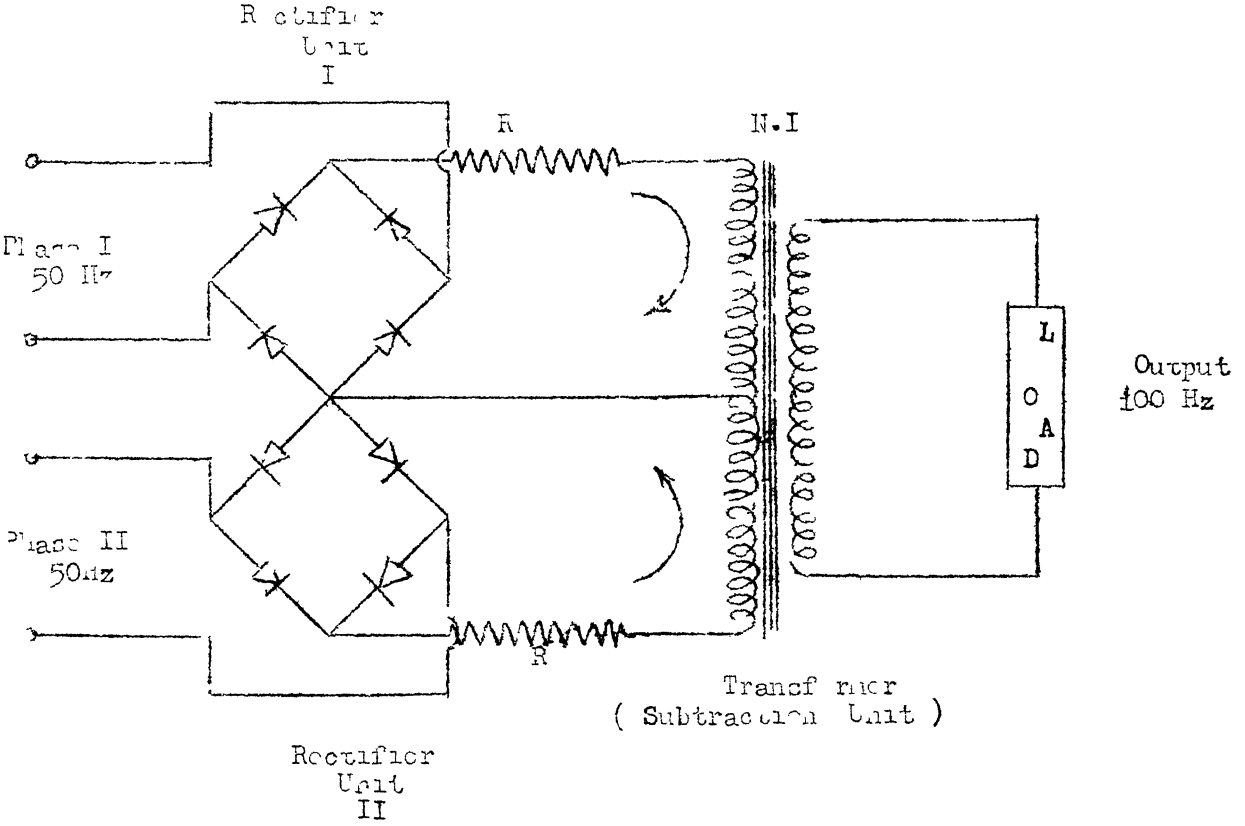


Fig.2.3 Frequency Doubler using Diodes and Magnetic Subtraction

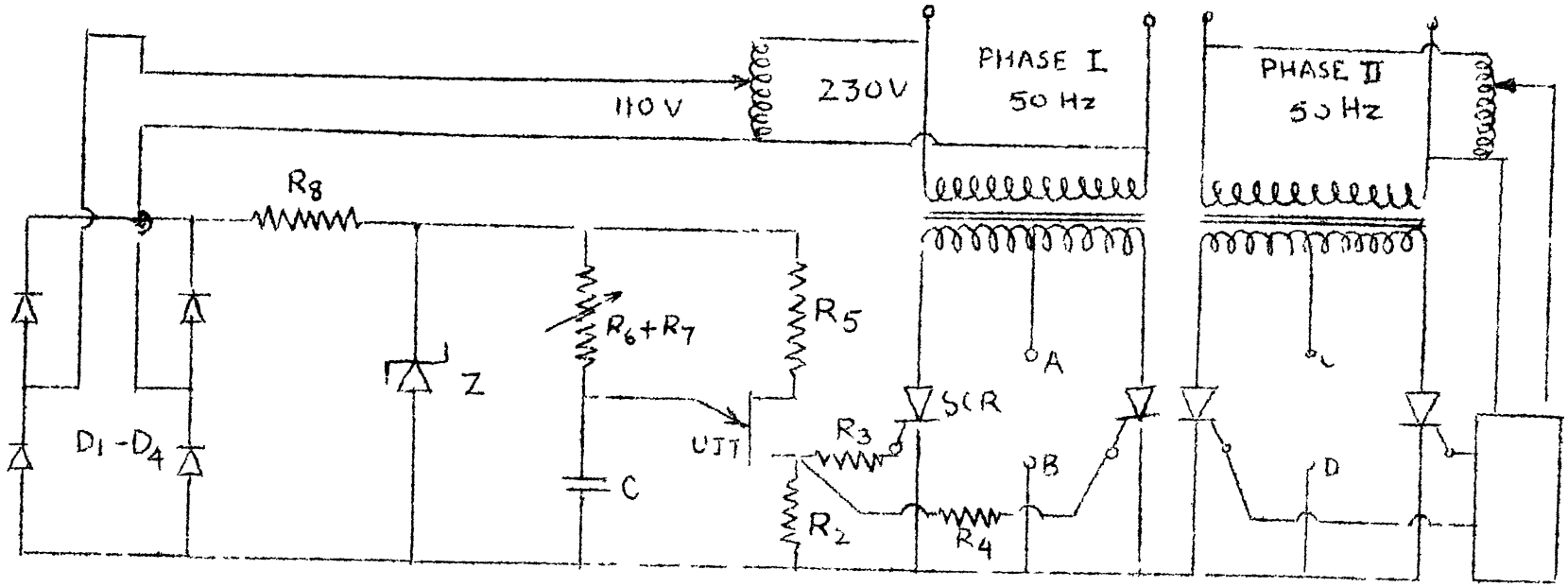
in the circuits arise due to the methods used for the subtraction of the two rectified signals and for the control of output voltage

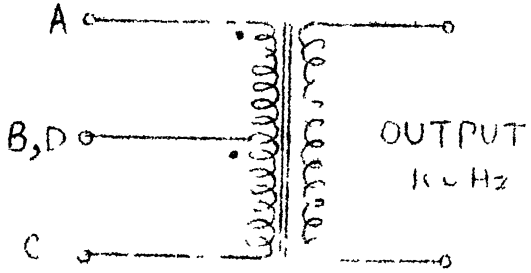
2.31 Circuits with magnetic subtraction :

A transformer with centre tapped primary is used as the subtraction unit The complete circuit is given in Fig 2.3. The ampere turns of the two halves of the primary winding are in opposite sense and hence the flux set up in the core will be due to the net ampere turns. The D.C. ampere turns being equal and opposite do not contribute to the core flux Due to the cancellation of D C. ampere turns, the turns ratio gets reduced by a factor two The two halves of the primary winding have to carry a large D.C. as the transformer winding resistance is usually quite small That is why two equal resistances have been added in series with the two halves of the primary winding. This affects the efficiency and the regulation of the circuit very badly. Instead of using resistances, a resistor R in the common lead can be used. This resistance besides controlling D.C. output also affects the output voltage waveshape as explained later.

The magnitude of double frequency output voltage can be controlled by

(1) varying the magnitude of the input voltages.





$D_1 - D_4$	—	IN4005
Z	—	3Z15A
SCR	—	2N1597
UJT	—	2N2646
C	—	0.1 μf

R_2	— 47 Ω, ½ W
R_3, R_4	— 22 Ω, ½ W
R_5	— 430 Ω, ½ W
R_6	— 33 K, ½ W
R_7	— 250 K LIN POT
R_8	— 33 K 5 W

GATE CONTROLLED FREQUENCY DOUBLER

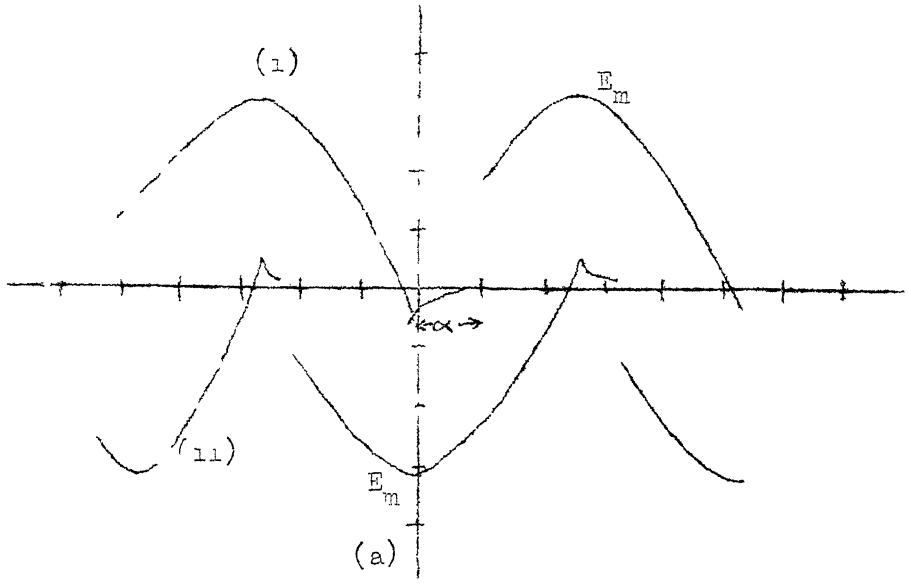
(ii) varying the phase shift between the two input voltages. This requires the use of a phase shifter

(iii) In case SCRs are used, the output voltage magnitude and waveshape can be controlled by controlling the firing instants of the SCRs The circuit used is shown in Fig.2.4, the design of gate circuit has been given in detail in Chapter III . The waveforms to be subtracted are shown in Fig.2.5(a) and the resultant output in Fig.2.5(b).

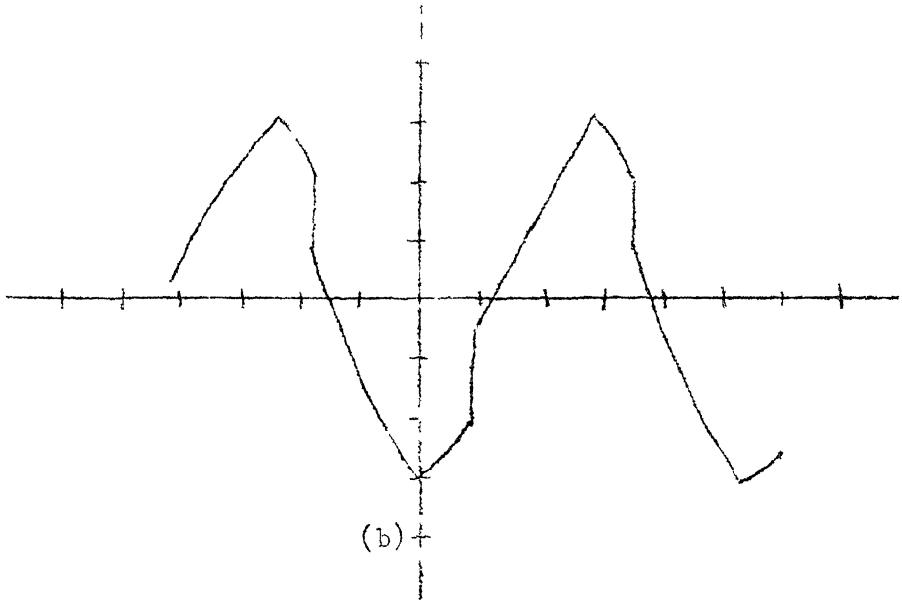
(iv) varying the resistance placed in the common lead to control the d.c. current, the diodes can be made to turn off at a desired instant depending upon the ratio of the load resistance and the resistance in the common lead. More will be discussed about this in a later section.

2.32 Electrical Subtraction

Two equal resistors are used for this purpose. This besides controlling the current through the rectifiers will also provide the difference of the two voltages appearing across them The arrangement is shown in Fig.2.6(a). The output voltage depends upon the ratio of R_L and R. The delta formed by the resistors R, R and R_L can be converted to an equivalent star with resistances R_1, R_1 and R_2 as shown in Fig 2.6(b),



Output of Rectifier Units



Output of Subtraction Unit

Fig.2.5

where

$$R_1 = \frac{R\,r_L}{2R+R_L}$$

and

$$R_2 = \frac{R^2}{2R+R_L} \qquad \text{also} \qquad \frac{R_1}{R_2} = \frac{R_L}{R}$$

The presence of R_2 affects the period of conduction of the diodes in both the rectifier units. When both the supply voltages are applied to the circuit, the voltage drops in R_1 and R_2 in each loop should sum up to the applied voltage. This condition gets automatically satisfied by the current adjustment in each loop. But when the voltage drop in R_2 itself equals the output of any of the rectifier unit, that rectifier unit stops conducting. The rectifier will continue to be in the non-conducting state as long as the voltage drop in R_2 exceeds the applied voltage. This phenomenon has been explained in Fig 2.7(a) and Fig 2.7(b).

The rectifier unit I will be 'off' ($i_1 = 0$) when

$$E_m \sin\theta \frac{R_2}{R_1+R_2} \geqslant E_m \cos\theta$$

or

$$\tan\theta \geqslant \frac{R_1+R_2}{R_2}$$

where 2θ is the period for which the rectifier unit remains conducting in a half cycle.

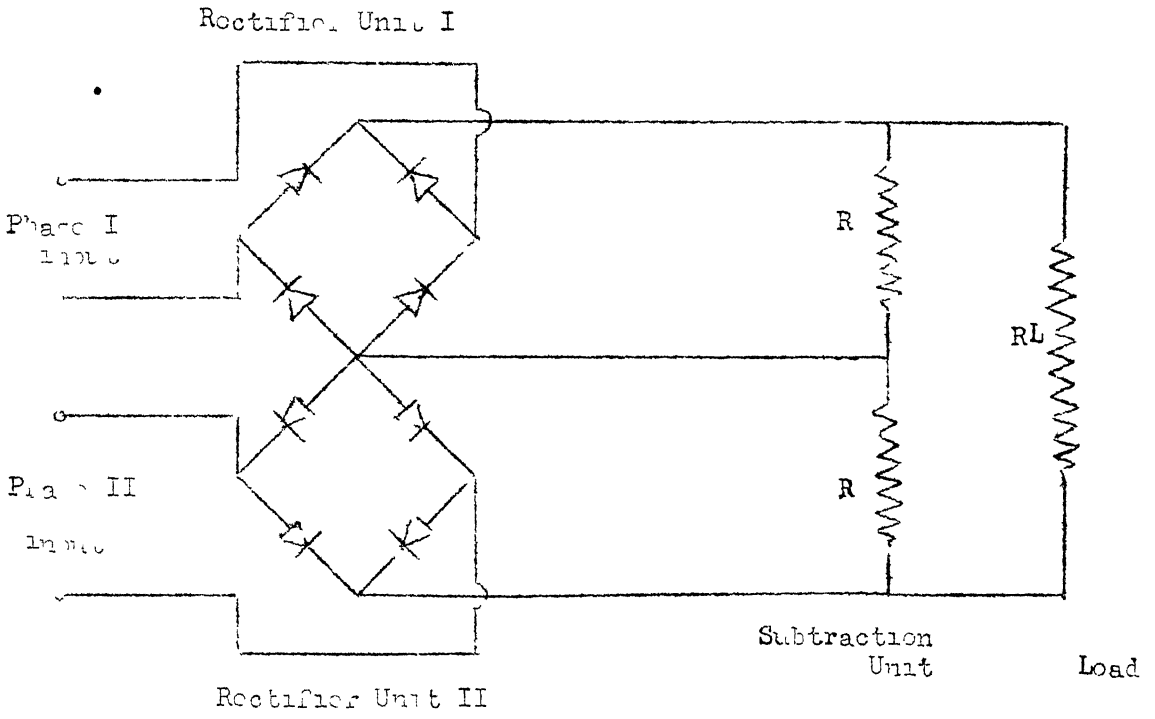


Fig. 2.6 a Frequency Doubler using diodes and employing Electrical subtraction

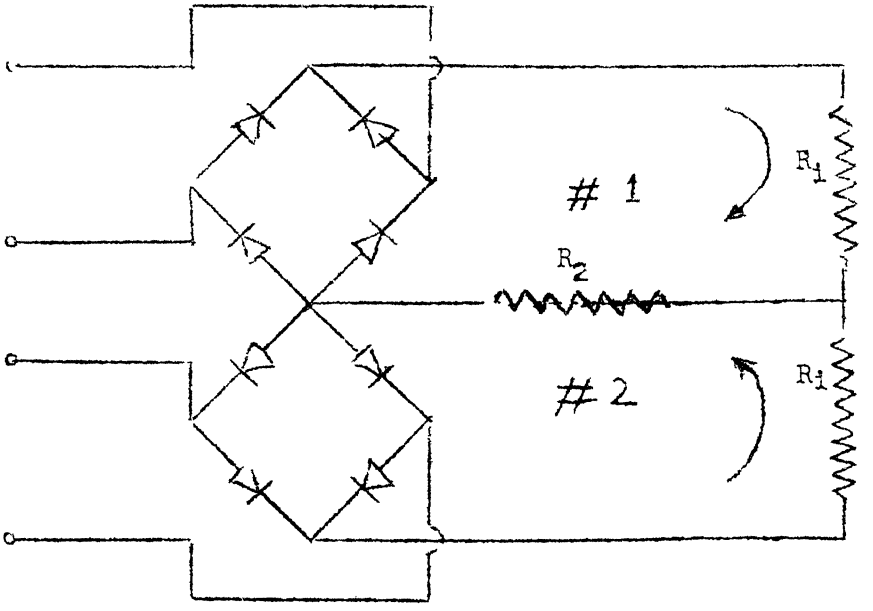
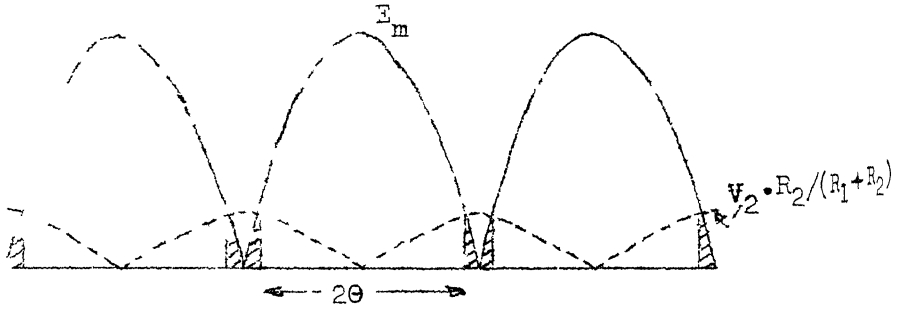
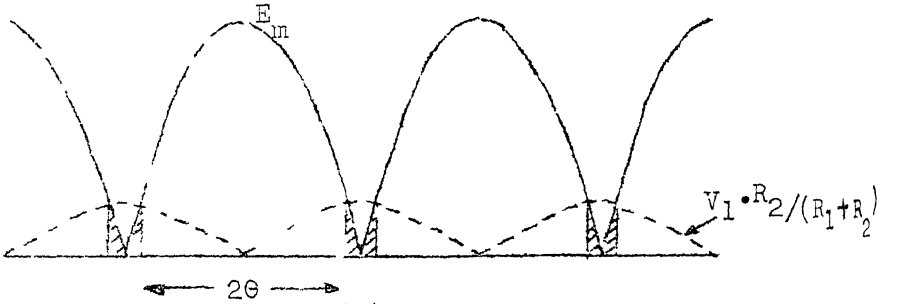


Fig.2.6(b) Equivalent Circuit of fig.2.6(a)



(a)



(b)

Fig. 2.7

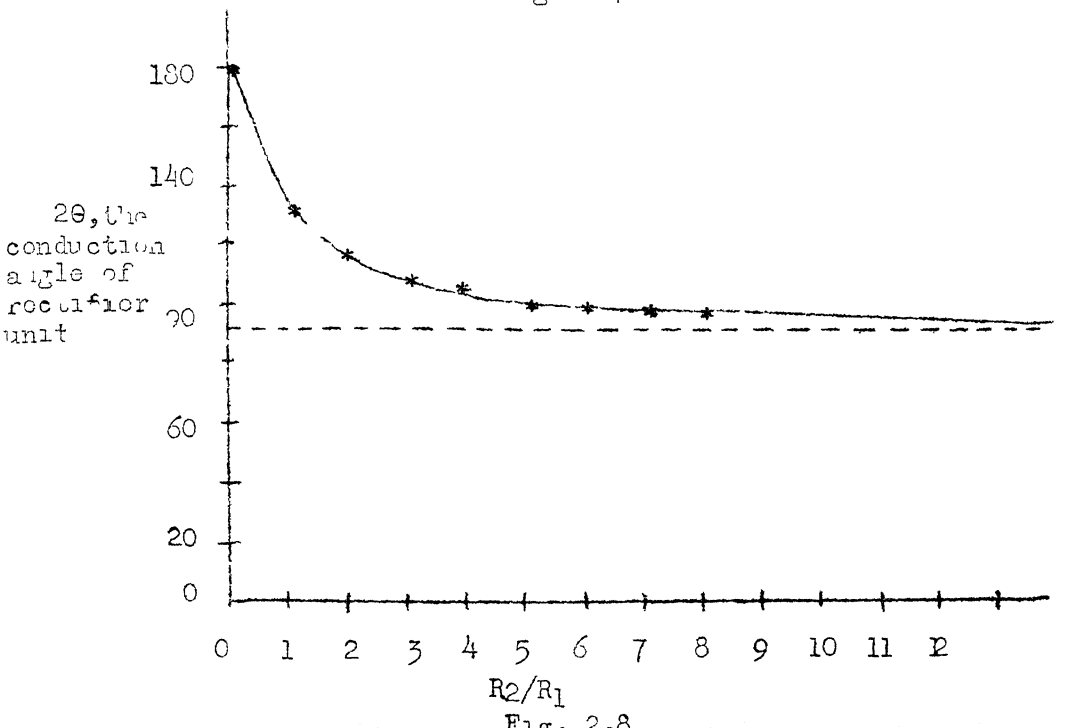


Fig. 2.8

Similarly rectifier unit II will be 'off' ($i_2 = 0$) when

$$E_m \cos \phi \frac{R_2}{R_1 + R_2} \geqslant E_m \sin \phi$$

or

$$\cot \phi \geqslant \frac{R_1 + R_2}{R_2}$$

but $\phi = 90 - \theta$

$$\therefore \quad \tan \theta > \frac{R_1 + R_2}{R_2}$$

The values of the conduction angle 2θ for different ratios of R_2/R_1 or R/R_L have been plotted in Fig.2.8. The conduction angle varies between 90° and 180°. It is 90° when $R/R_L = R_2/R_1 = \infty$ and 180° when $R_2/R_1 = R/R_L$ equals zero. Incidentally the dependence of the angle of conduction on R_2 or R_L provides us with a method to plot the regulation characteristic of this circuit.

2.4 Harmonic Analysis

The following harmonic analysis refers to the case of the gate controlled frequency doubler using magnetic subtraction.

In the voltage waveforms of Fig.2.5(a), α is the angle at which the rectifier goes into conduction.

If $f^{(1)}(\theta)$ and $f^{(11)}(\theta)$ be the functions representing the rectified voltage waveform (1) and (11) respectively, then

$$f^{(1)}(\theta) = a_o^{(1)} + \sum_{n=1}^{\infty} (a_n^{(1)} \cos n\theta + b_n^{(1)} \sin n\theta) \quad \ldots (a)$$

and $$f^{(11)}(\theta) = a_o^{(11)} + \sum_{n=1}^{\infty} (a_n^{(11)} \cos n\theta + b_n^{(11)} \sin n\theta) \quad \ldots (b)$$

Subtracting (b) from (a),

$$f(\theta) = f^{(1)}(\theta) - f^{(11)}(\theta)$$

Since $a_o^{(1)} = a_o^{(11)}$

$$\therefore f(\theta) = \sum_{n=1}^{\infty} (a_n^{(1)} - a_n^{(11)}) \cos n\theta + (b_n^{(1)} - b_n^{(11)}) \sin n$$

The magnitude of the nth harmonic will be given by

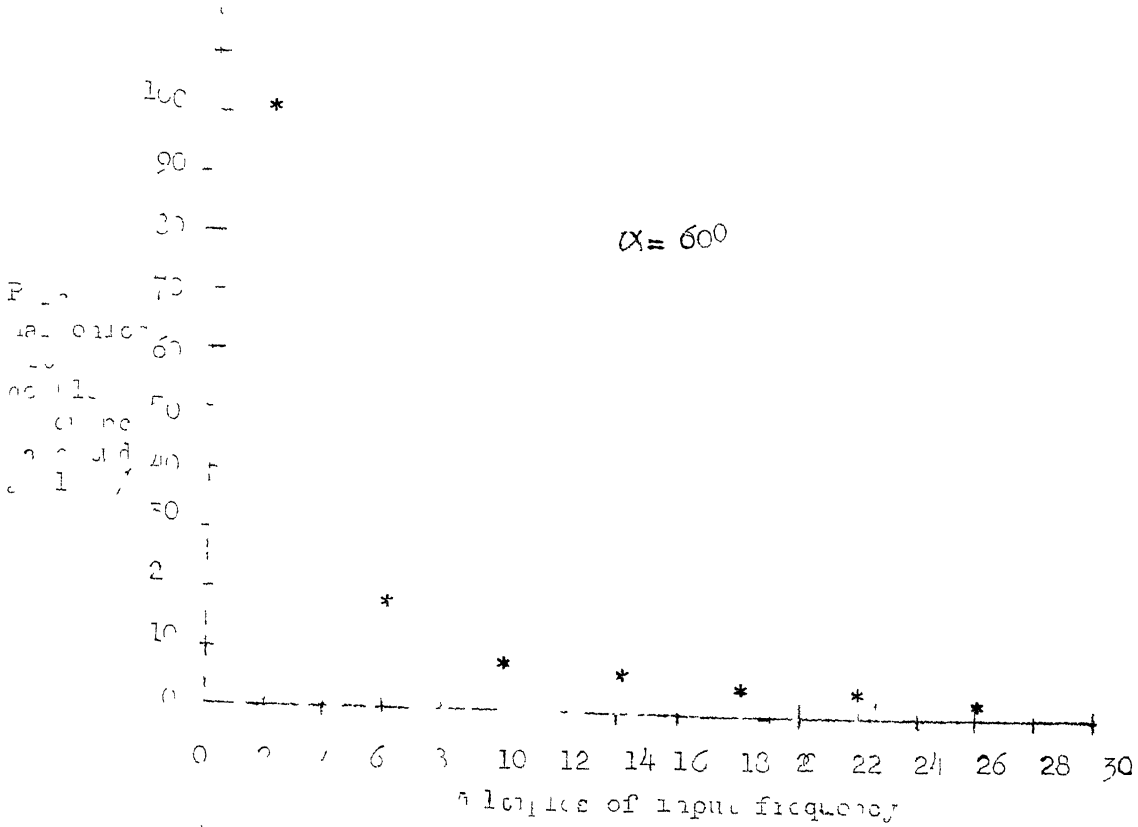
$$\sqrt{\left[a_n^{(1)} - a_n^{(11)}\right]^2 + \left[b_n^{(1)} - b_n^{(11)}\right]^2}$$

Since magnetic subtraction is used, the output r.m.s. voltage gets halved in a 1:1 transformer subtraction unit

$\therefore$ R.M.S. output voltage

$$= \frac{\sqrt{\left[a_n^{(1)} - a_n^{(11)}\right]^2 + \left[b_n^{(1)} - b_n^{(11)}\right]^2}}{2} \quad \ldots (A)$$

The expressions for $a_n^{(1)}$, $a_n^{(11)}$ and $b_n^{(1)}$ and $b_n^{(11)}$ have been given in Appendix 1.1. Using the expression (A) the magnitude of harmonics in the output of the frequency doubler can be found out for various firing angles. The Fig.2.9 gives the plot of % harmonics versus the multiples of the double frequency output.



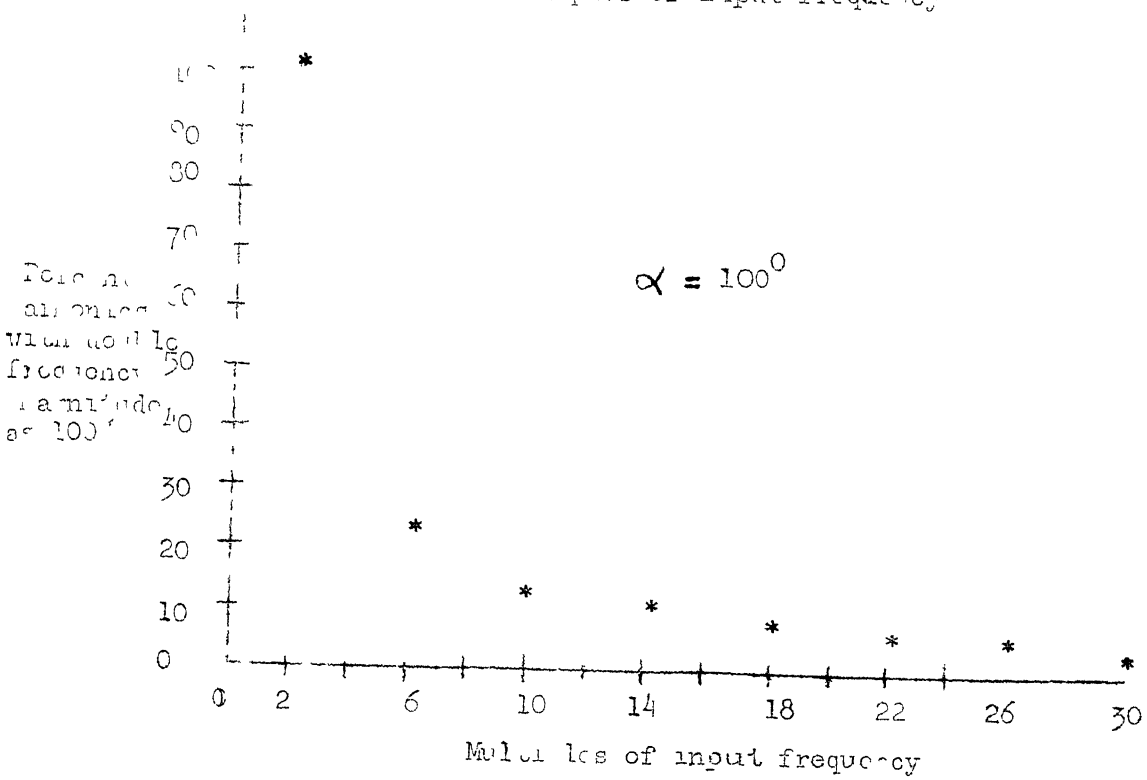


Fig.2.9 Harmonics Plot

2 5 Conclusions ·

The efficiency and regulation of the circuit were found to be extremely poor This is due to the presence of resistors in the diode circuit The efficiency of the circuit discussed in Section 2 32 was found to be of the order of 10% The usefulness of the circuit gets diminished only because of the presence of d.c. in the two halves of the subtraction unit. It may appear that the insertion of capacitors in place of resistors is a feasible solution for avoiding d c , but both the rectifiers stop conducting once the capacitor gets charged to the peak voltage and the circuit ceases to work. Thus it is found impossible to improve this circuit using electrical or magnetic subtraction units

CHAPTER III

AN IMPROVED FREQUENCY DOUBLER CIRCUIT

3.1 Introduction

The major drawbacks in the circuits discussed in the last chapter were due to the loss in D C limiting resistances in the subtraction unit. This loss has been avoided in the circuit discussed in this chapter by deleting the subtraction unit

3 2 Principle and Circuit Operation :

The block diagram of Fig.3.1 illustrates the principle involved. Two full-wave controlled rectifier units feed a common load such that their directions of feed are opposite to one another. SCRs have been used in the rectifier units to avoid a short circuit of the two phases at every instant of a cycle. Figs 3.2(a) and 3.2(b) show the circuit arrangements used Both circuits are identical so far as their performance and analysis are concerned

The linear reactors are placed in the lines to limit short circuit current, when more than one SCR conducts. The SCRs are fired in sequence 1 2 3 4 1 by pulses derived from the gate circuit Each pulse firing of the gates occur after a 90° interval.

Two modes of operation are possible. But only mode I operation will be discussed Since in Mode I,

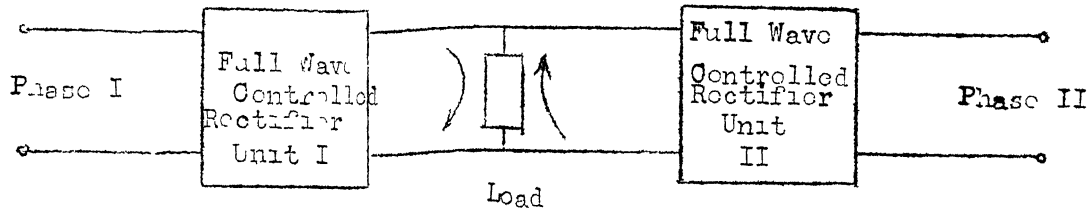


Fig.3.1 Block Diagram of a Improved Frequency Doubler Circuit.

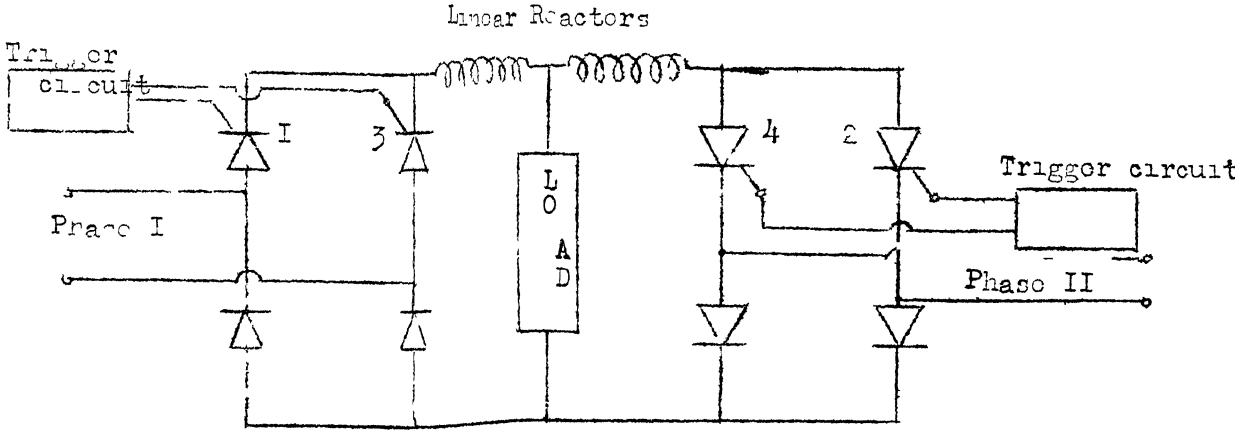
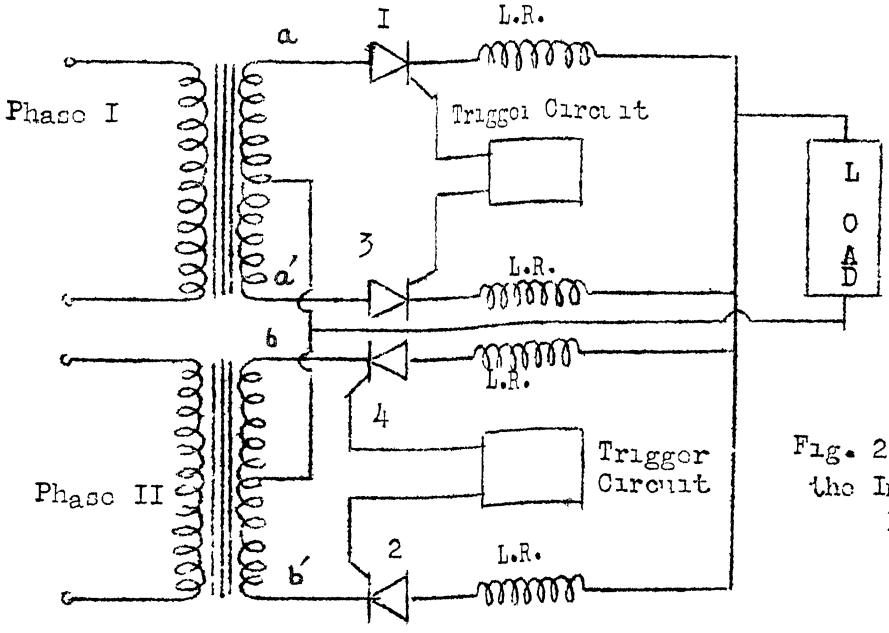


Fig. 3.2(a) An Improved Frequency Doubler Circuit



L.R—Linear Reactors

Fig. 2.3(b) Another Form of the Improved Frequency Doubler Circuit.

only one SCR conducts at a time, the use of linear reactors is unnecessary

For a purely resistive load, mode I operation occurs for firing angle θ lying between 0° and 90° and the output power can be varied by controlling the firing angle. Fig.3.3(a) and Fig.3.3(b) show the output voltage waveform for two different firing angles

For an inductive load, the mode I range of operation of the frequency doubler circuit gets reduced. This is because the current lags the voltage in an inductive circuit and the SCR continues to conduct until the current through it almost falls to zero. For a purely inductive load, this range is $45^{\circ} < \theta < 90^{\circ}$.

In mode I operation, the circuit analysis is very simple as the circuit reduces to a simple L-R circuit.

3.3 Gate Circuit, Operation and Design :

The circuits used for producing pulses to fire the SCRs are two relaxation oscillators using unijunction transistors (a negative resistance device). To have synchronisation of the pulses with the supply, the inputs to these relaxation oscillators are derived from the two phases

3.31 Operation :

Fig.3.4 represents a basic relaxation oscillator. A full wave rectified signal obtained from a rectifier

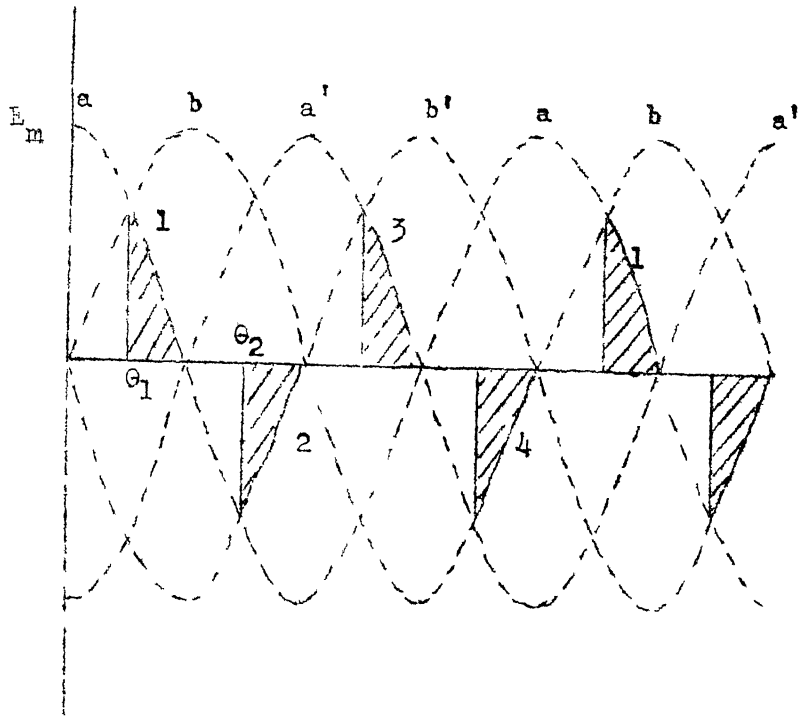


Fig. 3.3(a) Mode I Operation

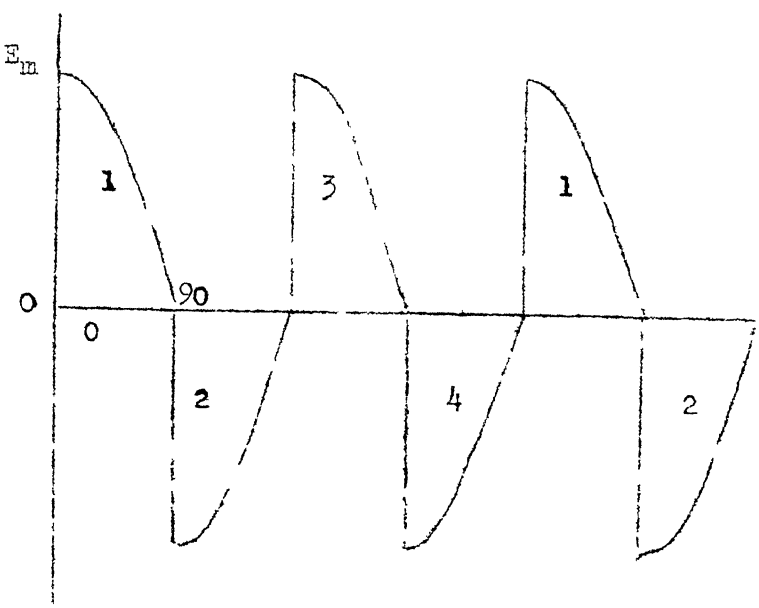


Fig. 3.3 (b) Output voltage waveform for $\theta = 0$
(Resistive Load)

bridge is used to supply both power and synchronising signal to the trigger circuit The zener diode is used to clip and regulate the peaks of A.C. as shown in Fig 3 6(c)

The circuit works as an oscillator because the emitter input characteristics of the UJT has a negative resistance region as indicated in Fig 3 5. The wave shapes of the circuit are shown in Fig.3.6. When the voltage across zener diode is applied, the capacitor C starts to charge exponentially towards the charging voltage as shown in Fig 3.6(c) through R_6 and R_7. The charging interval corresponds to the operation along path AB of the emitter characteristics shown in Fig.3.5. The emitter is reverse biased during charging interval so that input current I_E is very low. When the emitter voltage reaches the peak point, the emitter becomes forward biased and the dynamic resistance between the emitter and the base one drops to a low value. The input current I_E abruptly rises along path BC to a value equal to the peak point voltage Vp appearing on the capacitor C divided by emitter-to-base-one saturation resistance plus R_2. The capacitor now begins to discharge until the valley point is reached At this point the emitter ceases to conduct so that emitter current drops to that of A, which is the starting points for next cycle of operation.

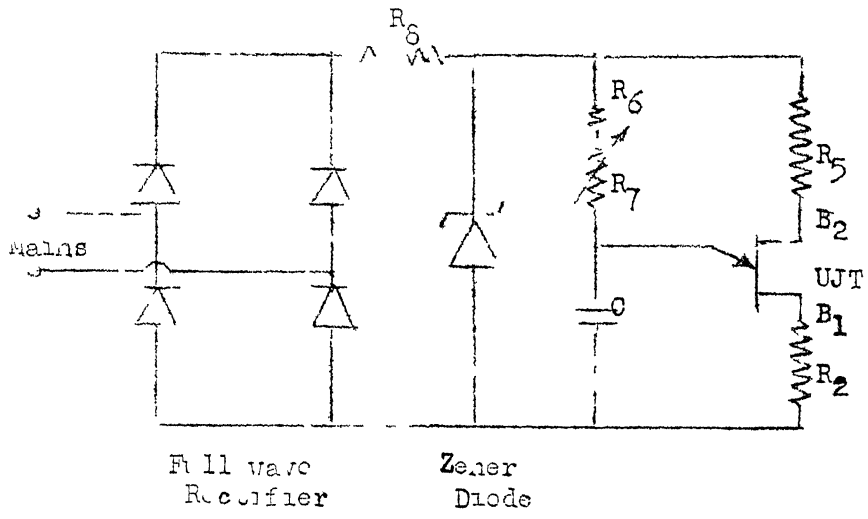


Fig.3.4 Relaxation Oscillator

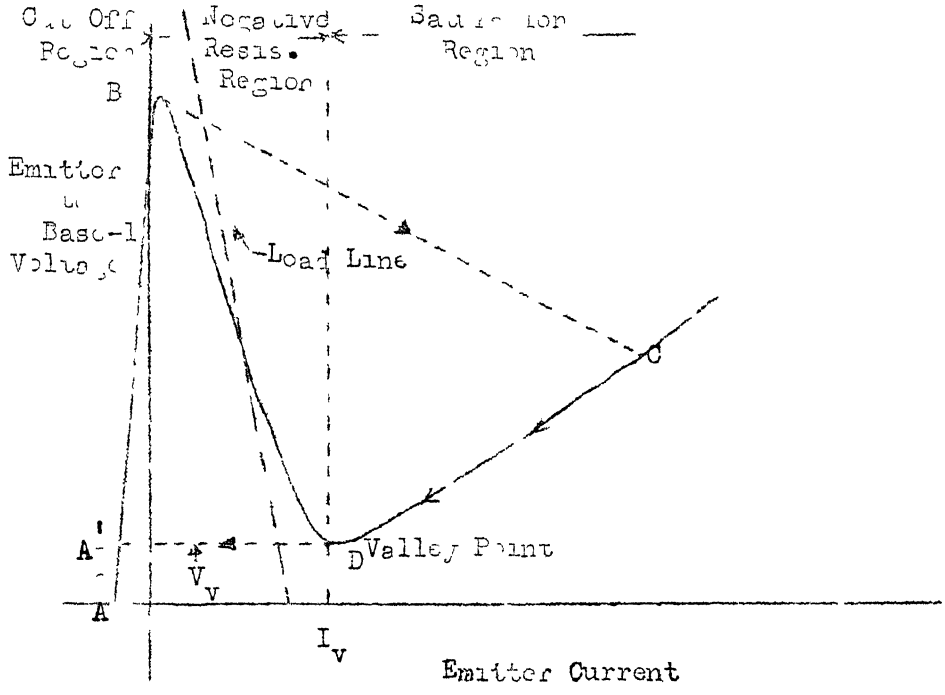


Fig.3.5 Static Emitter Characteristic Curve

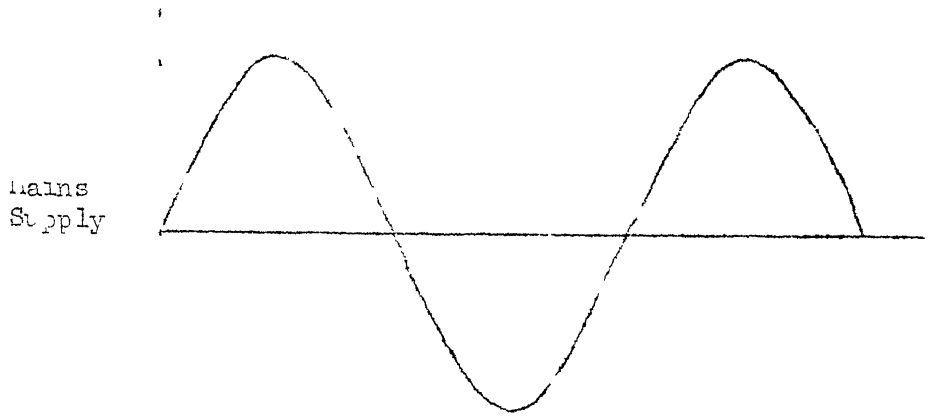
Depending upon the value of R_6, R_7 and C, a number of pulses may be produced in one half cycle of the line voltage. But in firing the SCR only the instant of occurance of first pulse is important At the end of each half cycle, the voltage at base two of the UJT will drop to zero and any charge on the capacitor will forward bias the emitter-base-one junction of UJT into conduction. The capacitor voltage becomes zero at the end of each half cycle thus synchronising the triggering pulses with the line voltage.

3 32 Design of the Triggering Circuit .

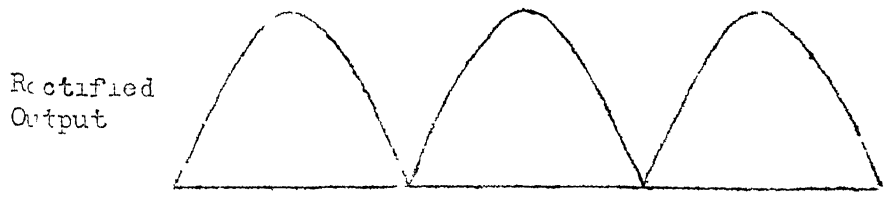
Specifications of UJT 2N2646

Absolute maximum ratings at 25°C

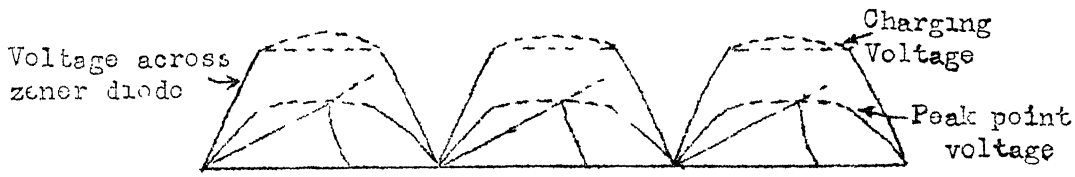
Power dissipation . . .	300 mw derate 3.0 mw/°C		
RMS emitter current .	50 mA		
Peak emitter current	2A (10 micro-farad or less discharge or 30V or less)		
Interbase voltage .	35 volts		
Operating temperature range .	-65°C to 125°C		
Intrinsic stand off ratio . η	Min. 0.56	Typ. 0.65	Max. 0.75
Interbase resistance (V_{BB}=3V, I_E=0) R_{BBO}	4.7K	7K	9.1K
Emitter saturation voltage V_{BB} = 10V, I_E = 50 mA V_E(Sat)		2V	
Peak point emitter current I_P V_{BB} = 25 V		0.4 μA	5 μA


Mains
Supply

(a)


Rectified
Output

(b)


Voltage across
zener diode
Charging
Voltage
Peak point
voltage

(c)


Pulse
Output

(d)

Fig. 3.6

Valley point current I_V 4 6 mA

V_{BB} = 20V, R_B = 100 ohms

Base 1 peak pulse voltage V_{OB1} 5.0 6.5 volts

In case of a UJT relaxation oscillator, wide range of circuit parameters are possible But some conditions for satisfactory operation must be satisfied

(1) Load line of $(R_6 + R_7)$ and V_{BB} must intersect the emitter characteristic curve to the right of the peak point. The condition ensures that the resistors $(R_6 + R_7)$ can supply sufficient current to the emitter to trigger UJT

$$\frac{V_{BB} - V_P}{R_1} > I_P \quad \text{where} \quad R_1 = R_6 + R_7$$

I_P is inversely proportional to V_{BB}

At 15 volts (voltage across zener diode)

$$\text{typical } I_P = \frac{0.4 \times 25}{15} \approx 0.7 \mu A$$

$$\text{maximum } I_P = \frac{5 \times 25}{15} \approx 8.3 \mu A$$

$$V_P = V_{BB} = 0.65 \times 15 = 9.75 \text{ volts}$$

$$\text{maximum } V_P = \max V_{BB} = 0.75 \times 15 = 11.25 \text{ volts}$$

Upper limit of R_1, taking into consideration the worst conditions i.e.

(a) the maximum value of V_P.

(b) the minimum value of V_{BB}

(c) the maximum value of I_P at minimum temperature of operation.

$$\therefore \quad \frac{15 - 11.25}{R_1} > 8.3\,\mu A$$

or $R_1 < 450$ K

(2) The load line formed by V_{BB} and R_1 must intersect the emitter characteristics to the left of the valley point.

$$\therefore \quad \frac{V_{BB} - V_v}{R_1} < I_v$$

If this condition is not satisfied the load line will intersect the emitter characteristics curve in the saturation region and the UJT may not turn off after it triggers on the first cycle.

V_v should be actually measured in the circuit as it depends upon R_{B1} and R_{B2}

Taking $V_v = 0.5\ V_{sat} = 0.5 \times 2 = 1$ V

and $I_v = 4$ mA (minimum value)

$$\therefore \quad \frac{15 - 1}{R_1} < 4 \text{ mA} \quad \text{or } R_1 > 3.5 \text{ K}$$

Thus $R_6 = 3.3$ K (fixed) and $R_7 = 250$ K (variable) have been chosen.

(3) The selection of C is governed by the emitter peak current, which should not increase above 2A, for values of $C < 10\ \mu f$ and peak point voltages < 30 V. For higher C (>10 uf) or higher voltages (>30V) a resistance in series with C should be used. This additional resistance should

be at least one ohm per microfarad of C Again the value of C should not fall below 0 001 uf for 2N2646 because the amplitude of emitter voltage waveform will decrease This decreases the frequency stability of the circuit and also reduces the allowable range of R_1

C = 0 1 microfarad has been selected

Control from 0° to 180° over the half cycle of line voltage is required. No pulse will be produced between 0 and θ_o, where θ_o is given by

$$15 = 110\sqrt{2}\ \text{Sin}\ \theta_o \quad \text{or} \quad \theta_o = 5.5^\circ.$$

5.5 degrees corresponds to 0.3 m.secs in this case, when input frequency is 50 Hz Thus control from 0.3 msecs to 10 msec is required.

Since R_1 = 3.3 K and C = 0 1 μf and if η = 0.63 then

$$T = \frac{1}{f} R_1 C \ln \frac{1}{1-\eta}$$

which gives T = 0.76 msec.

0.76 msec. correspond to 13.68 degrees. Therefore control over the half cycle can be had from 13.68° to 180° approximately.

R_5 is given by $\frac{0.7 R_{BB}}{V_1}$ which gives R_5 = 435 ohms for

V_1 = 15 V, R_{BB} = 7 K and η_{max} = 0.75

R_2 is limited to a value below 100 ohms, choosing

R_2 = 47 ohms

The complete specifications of the components used in the triggering circuit have been given in Fig.2.4, Chapter II.

3.4 Harmonics Analysis

The Fourier series representation of the output voltage waveform as given in Eqn 3.3(a) is

$$f(\theta) = a_0 + \sum_{n=1}^{\infty} (a_n \cos n\theta + b_n \sin n\theta)$$

The Fourier coefficients have been worked out in Appendix 3.1 Considering the limiting case of Mode I i.e., when $\theta_1 = 0^\circ$ and $\theta_2 = 90^\circ$,

$$a_n = \frac{E_m}{2\pi}\left[\frac{\sin(1+n)\pi/2}{1+n} + \frac{\sin(n-1)\pi/2}{n-1} + \frac{\cos(n+1)\pi}{n+1} - \frac{\cos(n+1)\pi/2}{n+1} - \frac{\cos(n-1)\pi}{n-1} + \frac{\cos(n-1)\pi/2}{n-1}\right]$$

It is found that $a_n = 0$ for n = 4, 8, 12, 16 . etc.

For other values of n, a_n can be calculated giving one part of the Fourier series as

$$f_1(\theta) = \frac{E_m}{\pi}\left[\frac{1}{2}\cos\theta + \frac{2}{3}\cos 2\theta - \frac{1}{2}\cos 3\theta + \frac{1}{6}\cos 5\theta + \frac{2}{35}\cos 6\theta - \frac{1}{6}\cos 7\theta + \frac{1}{10}\cos 9\theta + \frac{2}{99}\cos 10\theta - \frac{1}{10}\cos 11\theta + \frac{1}{14}\cos 13\theta \ldots\right]$$

and

$$b_n = -\frac{E_m}{2\pi}\left[\frac{\cos(n+1)\pi/2}{n+1} - \frac{1}{n+1} - \frac{1}{n-1} + \frac{\cos(n-1)\pi/2}{n-1} - \frac{\sin(n-1)\pi/2}{n-1} + \frac{\sin(n+1)\pi/2}{n+1}\right]$$

Here again, $b_n = 0$ for n = 4, 8, 12, 16 .... etc.

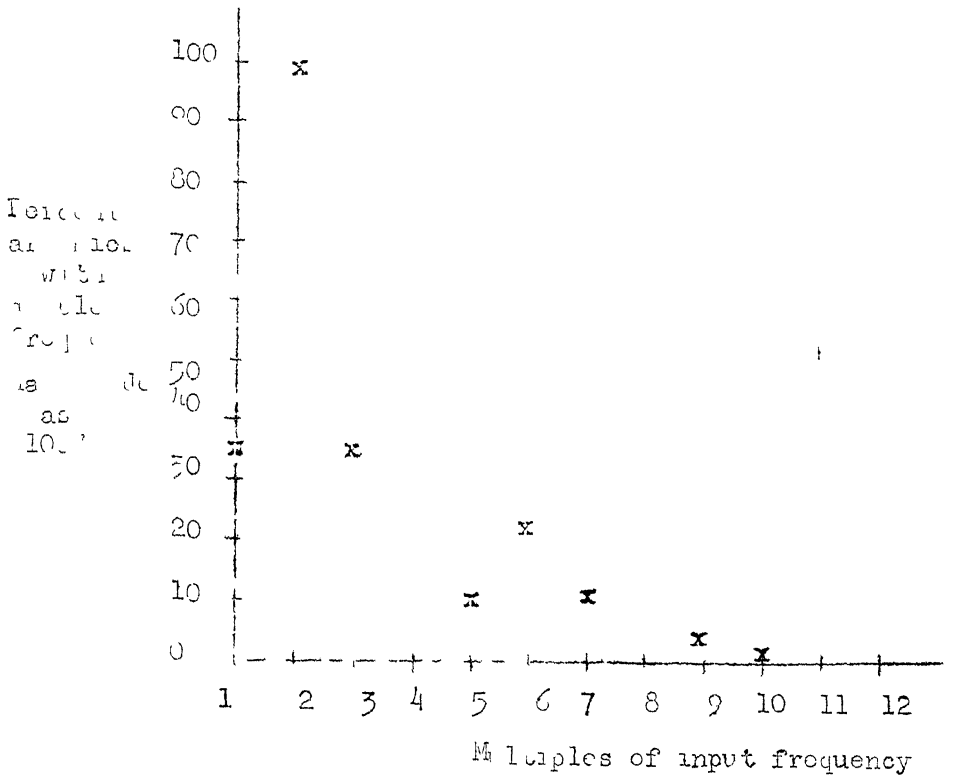
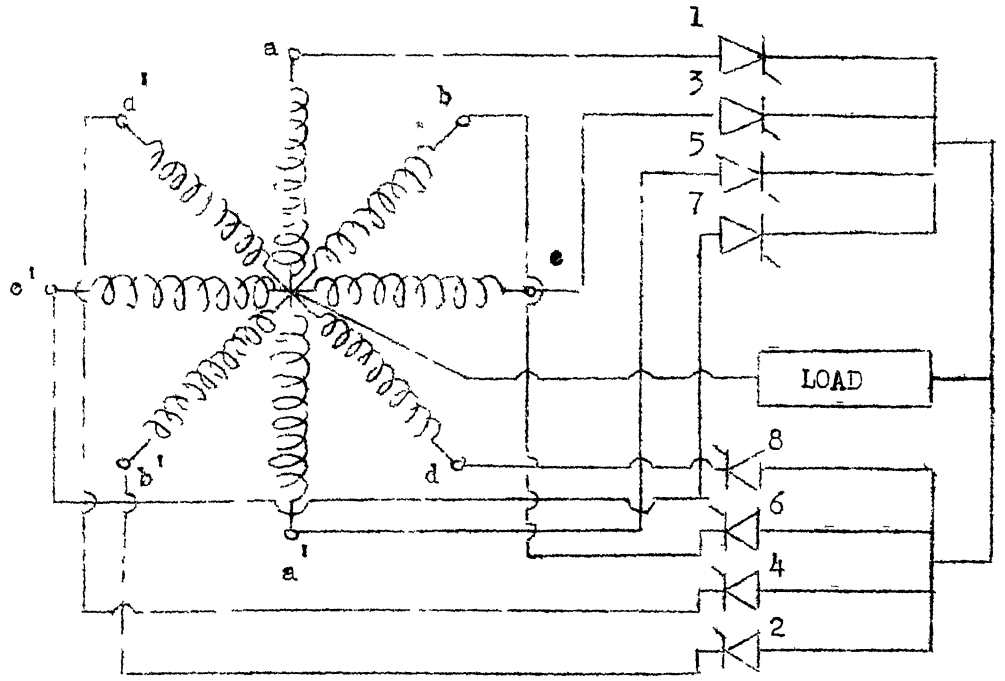


Fig. 3.7 Harmonics Plot



For other values of n, b_n can be calculated giving the other part of the Fourier series as

$$f_2(\theta) = \frac{E_m}{\pi}\left[\frac{1}{2}\sin\theta + \frac{4}{3}\sin 2\theta + \frac{1}{2}\sin 3\theta + \frac{1}{6}\sin 5\theta + \frac{12}{35}\sin 6\theta + \frac{1}{6}\sin 7\theta + \frac{1}{10}\sin 9\theta + \frac{1}{11}\sin 10\theta\right]$$

$$f(\theta) = \left[\frac{E_m}{2\pi}(\sin\theta + \cos\theta) + \frac{2}{3\pi}E_m(2\sin 2\theta + \cos 2\theta) + \frac{E_m}{2\pi}(\sin 3\theta - \cos 3\theta) + \frac{E_m}{6\pi}(\sin 5\theta + \cos 5\theta)\right]$$

The magnitude of the nth harmonic is given by $\sqrt{a_n^2 + b_n^2}$. Fig.3.7 shows the harmonic plot.

3.5 A General Frequency Multiplier

The principle employed for frequency doubling can also be used for producing higher even harmonics. To have a frequency multiplification by a factor n, where n is even, a 2n phase supply is required. Fig 3.8 shows the circuit for a four-fold increase in the frequency. The firing sequence of SCRs being 1 2 3 4 5 6 7 8 and 1. For operation in Mode I i.e., when only one SCR conducts at a time, no current limiting reactors are required. Fig.3.9 shows the output voltage waveform when the circuit operates in Mode I. A similar arrangement cannot be used for the generation of odd harmonics

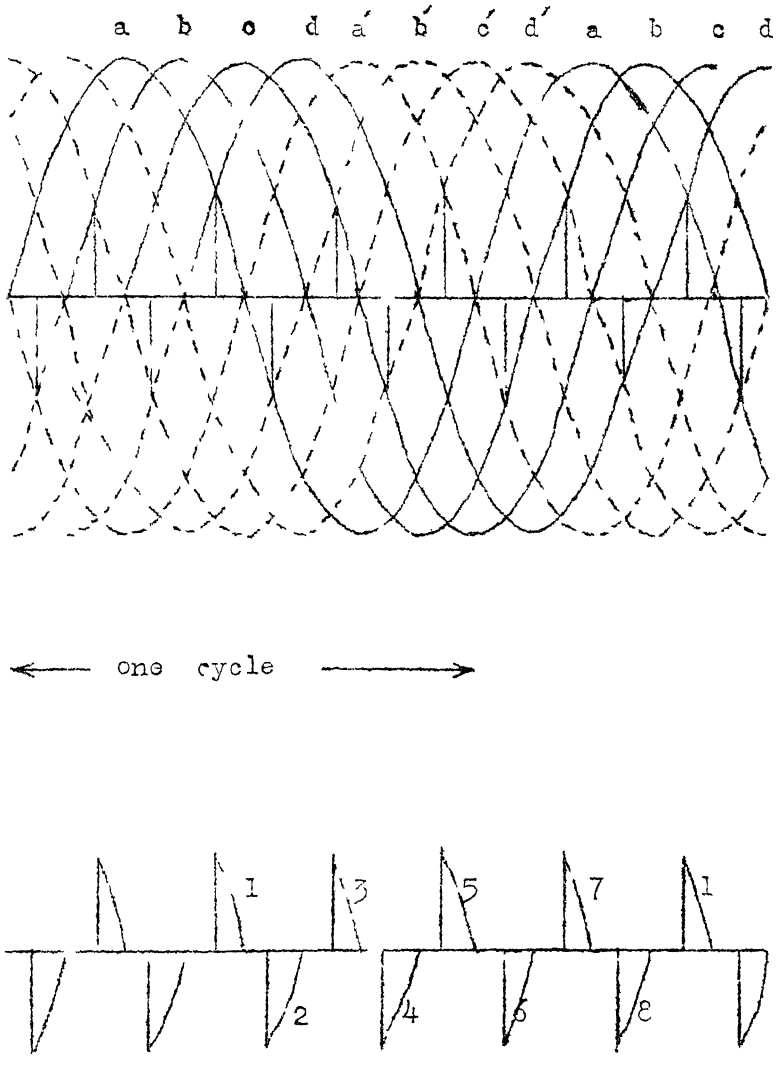


Fig 3.9 Output of Frequency Quadrupler

5.6 Conclusions

The improved frequency doubler discussed in this chapter has better efficiency and regulation as compared to those discussed in Chapter I But as far distortion is concerned, the output has higher harmonic contents. The same circuit can be used for generation of higher frequency output if suitable poly-phase balanced input is used.

CHAPTER - IV

FREQUENCY DOUBLER WITH SINGLE PHASE INPUT

4.1 Introduction :

The frequency doubler described in this chapter requires only a single phase input. The output is a half cosine wave and the transition from one peak to another is almost instantaneous. This transition is brought about by the use of a commutating capacitor like the one used in an inverter circuit.

4.2 Fundamental Circuit :

A switching analogy can be used to illustrate the frequency doubler action (Fig.4.1a). The switches S_1 and S_2 are such that both of them cannot remain'on' simultaneously. Turning 'on' of one say S_2 turns the other (S_1) switch 'off'. For frequency doubling, in the region A of the input voltage waveshape (Fig.4.1b), say S_1 is 'on' and S_2 'off' and in the region B, S_2 will be 'on' and S_1 'off'. The switch over from S_1 to S_2 and vice-versa is assumed to occur instantaneously thus avoiding any short circuit on the supply. The ideal output voltage waveform is shown in Fig.4.1(c).

4.3 Commutation :

The switches used in the analogy may be replaced by thyristors as shown in Fig.4.2. Each switch is replaced by two thyristors connected in anti-parallel so

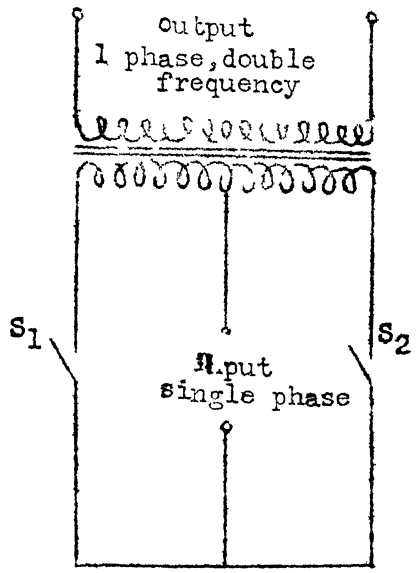


Fig.4.2(a) Switching analogy of Frequency Doubler

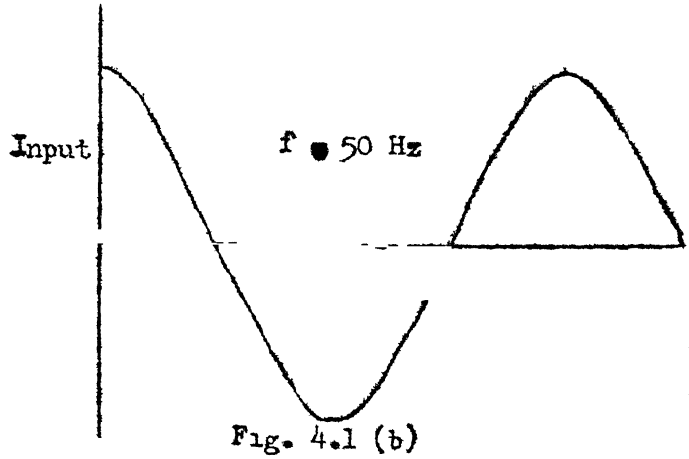


Fig. 4.1 (b)

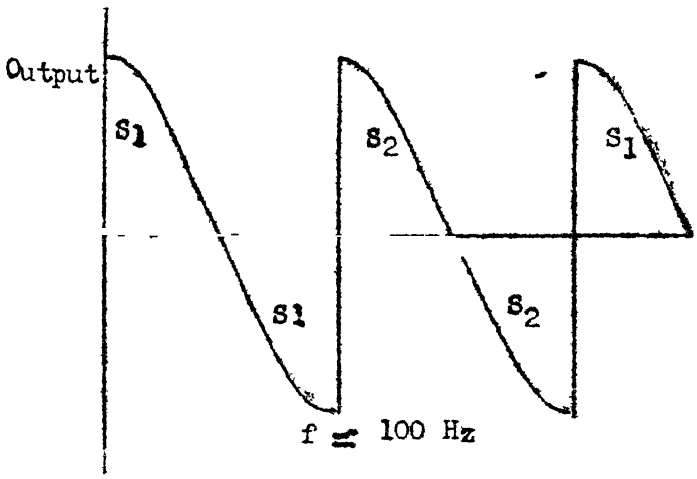


Fig. 4.1(c)

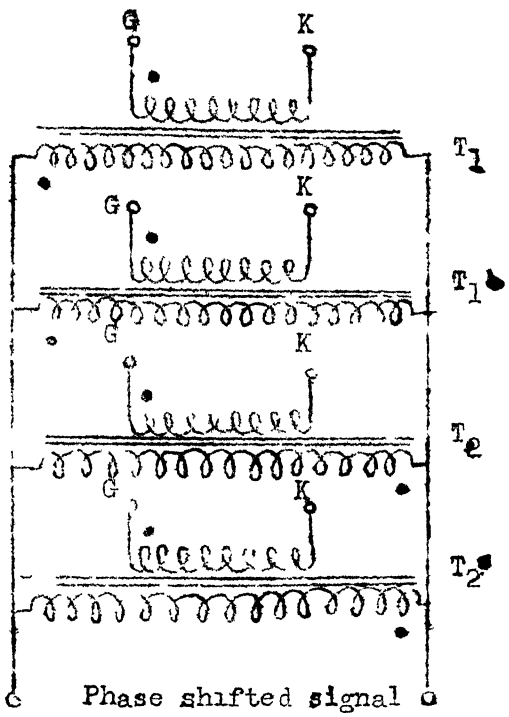


Fig.4.4 Isolating transformers connections

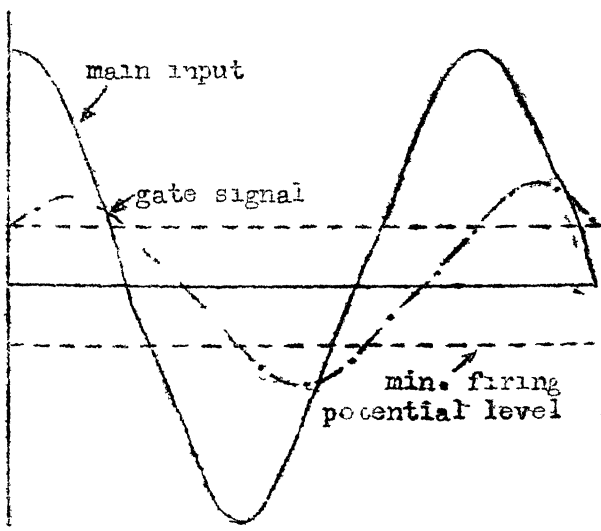
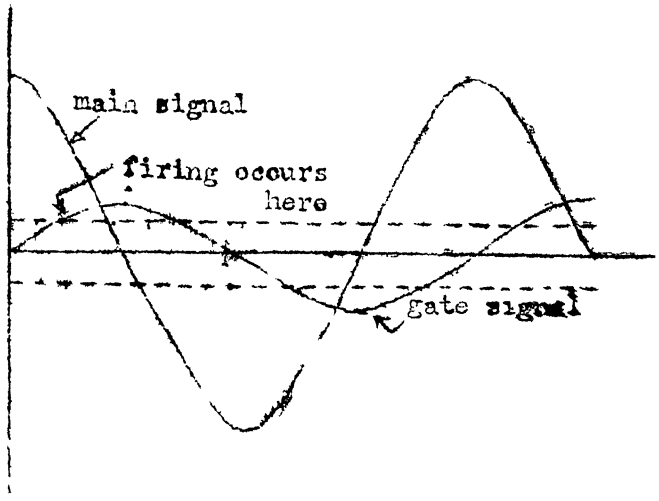


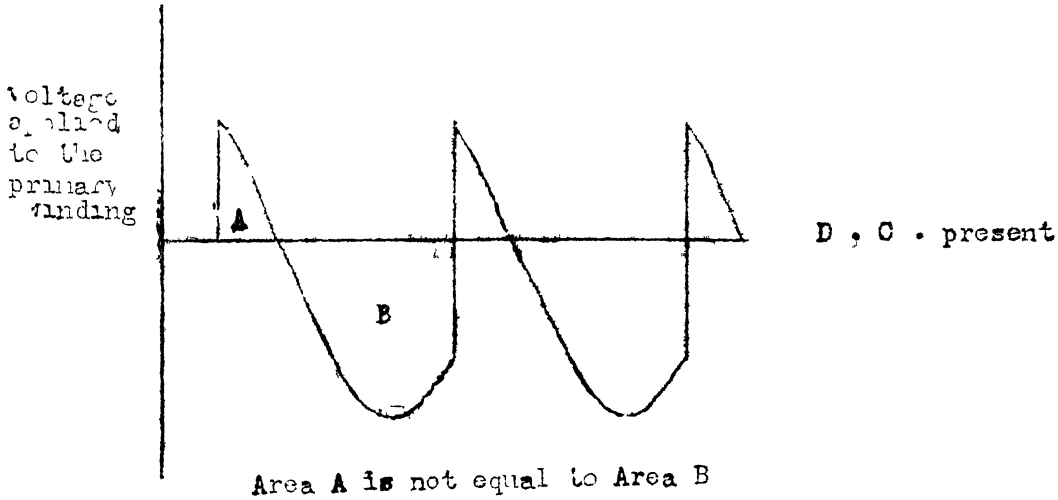
Fig.4.3

that one thyristor conducts for the positive quarter cycle and the other conducts for the following negative quarter cycle. The thyristors may be turned 'on' by a positive gate signal applied between the gate and the cathode when their anodes are positive w.r.t. the cathodes, but the turn 'off' of the thyristor during transition from S_1 to S_2 or vice-versa has to be accomplished by means of additional circuitry which acts to reduce current through the conducting thyristor to zero for a given length of time allowing it to cease conduction. This turn 'off' action is termed as commutation and it is defined as the transfer of current from one path to another. The energy for this commutation is stored in a capacitor C, called the commutating capacitor, which gets discharged at the instant of commutation to drive the thyristor current to zero for the required period, termed the turn off time, for the thyristor to recover its forward blocking capability. Since a thyristor takes some time (order of microsecs.) to turn 'off, during current transfer (commutation) two thyristors will conduct simultaneously thus placing a short circuit across the supply. To avoid this, a commutating inductance L is connected in series with the input voltage source.

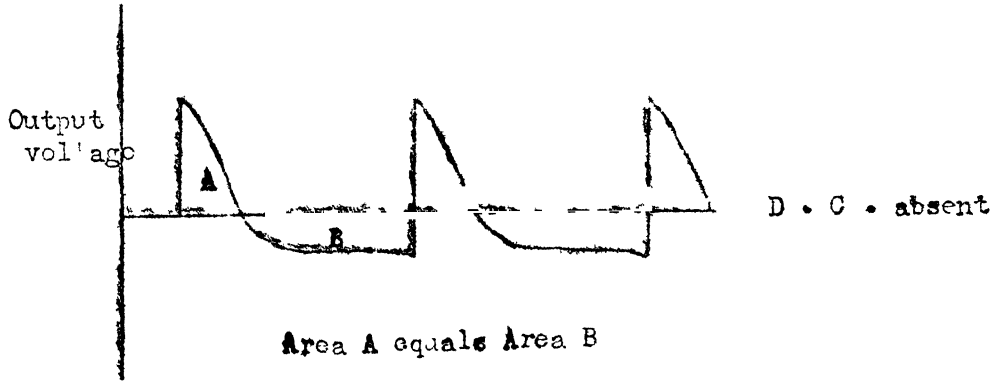
4.4 Gate Firing :

The voltage supplied to the gates of SCRs if of rectangular waveform is kept 90° out of phase with the



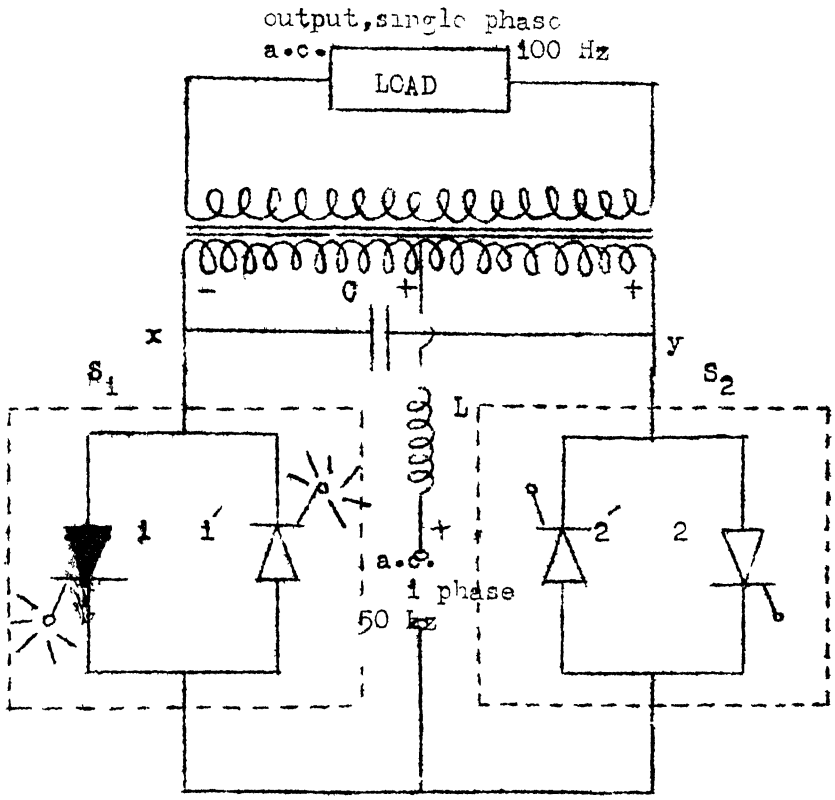


Area A is not equal to Area B



Area A equals Area B

Fig. 4.5



SCR 1 is ON

Fig. 4.2(a) Each Switch replaced by two SCRs connected in antiparallel

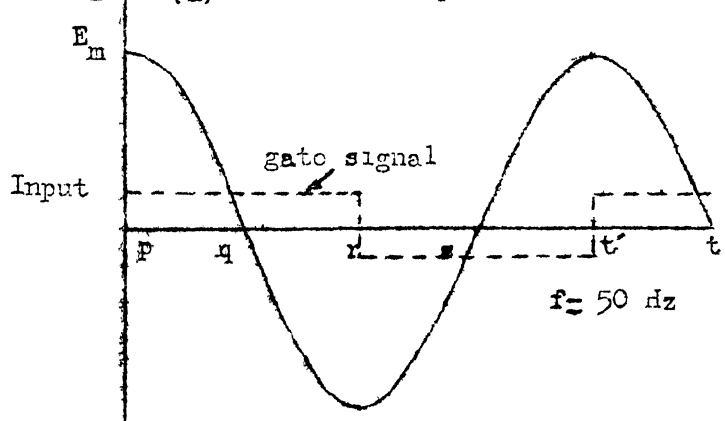


Fig. 4.2(B)

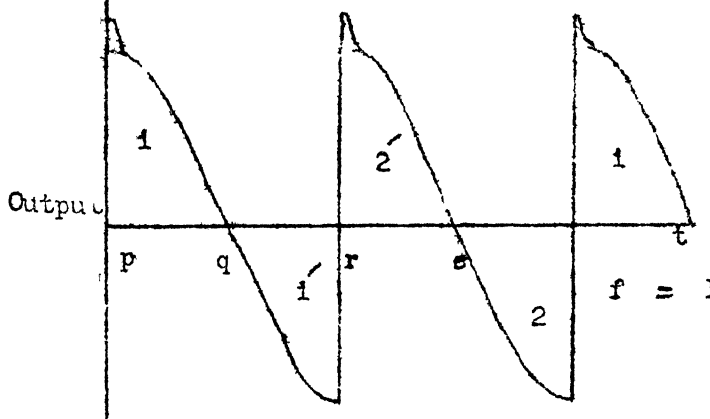


Fig. 4.2(C)

input voltage, because for a symmetrical double frequency output, the commutation should occur when the input is passing through its peak (Fig.4.2 B). To produce this phase shifted rectangular waveform from a sinusoidal signal will require some additional circuitry. To avoid this, a sinusoidal gate signal can be used with such a phase shift that the thyristors are able to fire when their anode voltages pass through their peaks (Fig.4.3). This phase shift in sinusoidal gating signal can be had by the use of a R-C phase shifting network as given in Appendix 4.1. This voltage is fed to the gates of the thyristors through isolating transformers. For region A indicated in Fig.4.1(b), the gates of SCRs 1 and 1' should be positive with respect to cathodes and for region B, the gates of 2 and 2' should be positive. The isolating transformers used are connected to the gates as shown in Fig.4.4.

In case, the firing does not occur when the input is passing through its peak, then the two halves of the double frequency output will have unequal time durations and the transformer primary winding will have to carry D C. (Fig.4.5).

4.5 Operation :

For each quarter of the input cycle, the circuit conditions will be discussed (refer Fig.4.2(B), (C)).

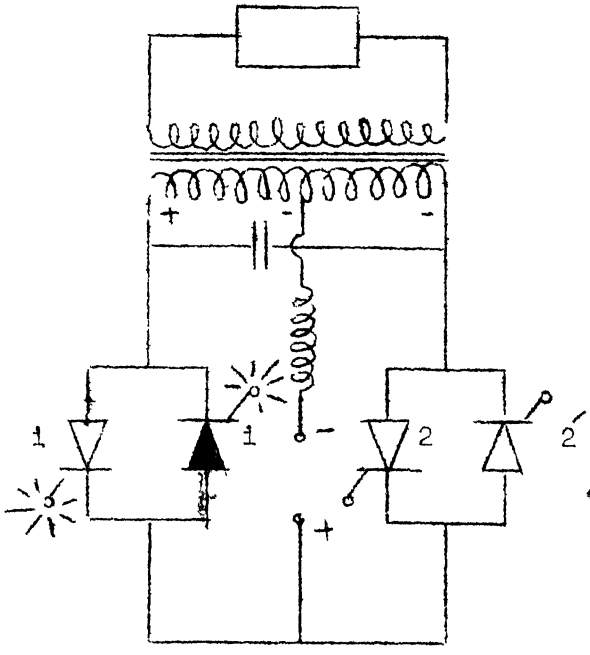
a) Resistive load :

In the first quarter of the input cycle (p-q) (refer Fig. 4.2), the gates of both 1 and 1' are positive but only SCR 1 conducts because of the positive supply to the anode of SCR 1. The voltage appearing across the capacitor is twice the voltage appearing across each half of the transformer primary winding.

In the second quarter cycle (q-r) the anode of SCR 1 becomes negative and that of SCR 1' becomes positive with respect to cathode. SCR 1 stops conducting and 1' goes into conduction. This commutation from 1 to 1' is natural because of the reversal of the applied voltage. SCR 1' conducts till the input passes through the negative maximum. The conditions in the circuit are indicated in Fig.4.6(a) for the quarter cycle (q-r).

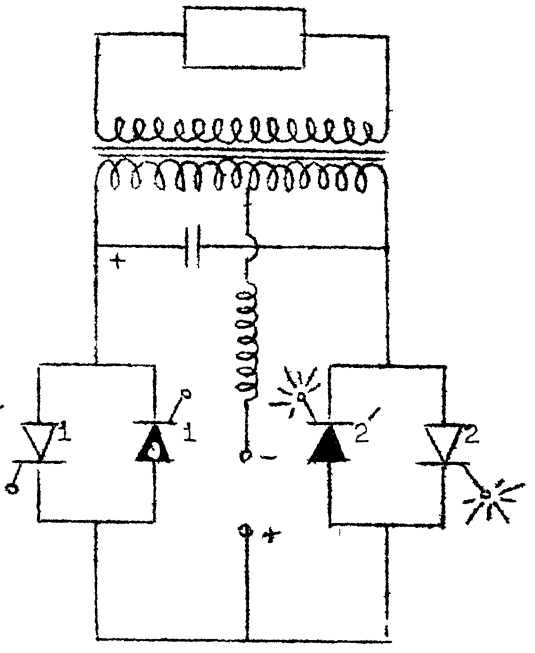
Commutating interval :

At the end of quarter cycle q-r, the voltage across capacitor is $2E_m$ with x at higher potential. The gates of 1 and 1' are no more having positive signals but instead the gates of 2 and 2' are positive. SCR 2' goes into conduction. Both 1' and 2' are shown conducting in Fig.4.6(b). This places a short circuit across the supply and capacitor also. The capacitor discharges through 1' and 2' turning off 1' and the excessive



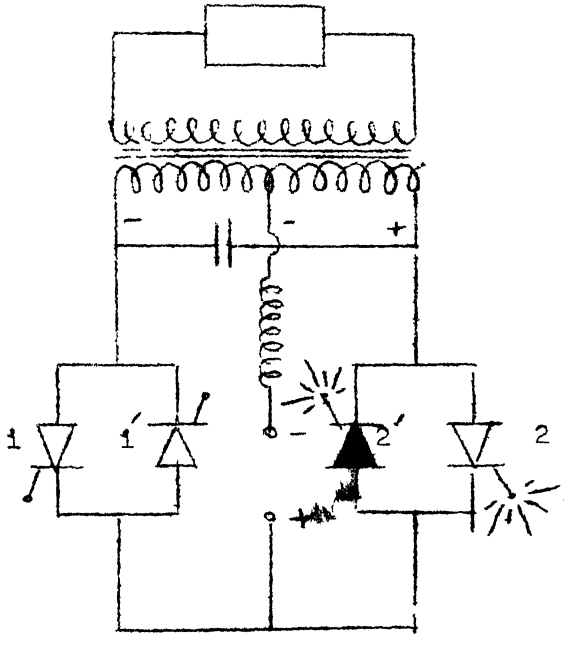
1 conducts During $\frac{1}{4}$ cycly q-r

(a)



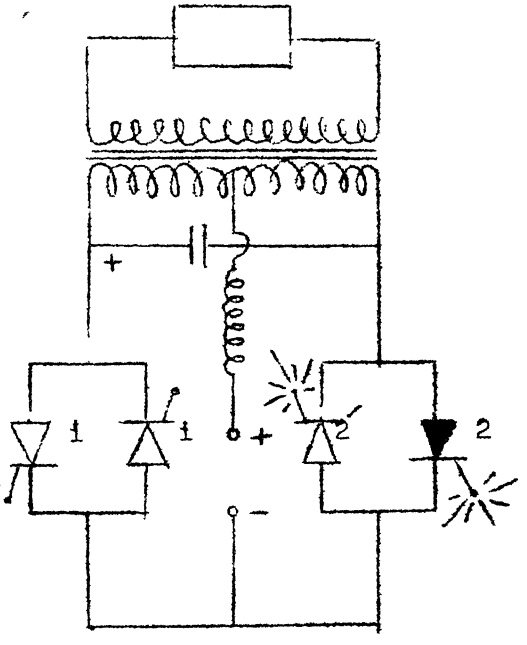
(b)

During Commutation, two SCRs conduct simultaneously



During $\frac{1}{4}$ cycle r-s SCR 2 conducts

(c)



During $\frac{1}{4}$ cycle s-t SCR 2 conducts

(d)

Fig. 4.6

capacitive energy discharges through the load. This gives rise to some oscillations in the load voltage waveform. SCR 1' gets turned 'off' only if the current pulse due to capacitor discharge exceeds the current carried by SCR 1' and lasts for a time long enough for SCR 1' to regain its forward blocking capability. Also care should be taken that the peak pulse current due to capacitor discharge does not exceed the surge forward current of SCRs. The choice of L and C depends upon the above factors. At the end of the commutating interval, the circuit conditions are shown in Fig. 4.6(c). SCR 2' conducts for another quarter cycle (r-s) At s the input voltage reverses and SCR 2' gets naturally commutated. SCR 2 starts conducting and keeps conducting till the input passes through its positive peak.

The current transfer from SCR 2 to SCR 1 will occur in the same way as it occured from SCR 1' to 2'.

b) Inductive load :

As shown in Appendix 4.2 the load current expression in case of inductive load is given by

$$i = \frac{E_m}{Z} \cos(wt-\theta) + \left(i(0) - \frac{E_m}{Z} \cos\theta \right) \cdot e^{\frac{-Rt}{L}}$$

where

$$\theta = \tan^{-1} \frac{wL}{R} \quad \text{and} \quad Z = \sqrt{R^2 + (wL)^2}$$

and $i(0) = \frac{E_m}{Z}\left(\frac{\cos(2\pi f \times 0.01 - \theta) - e^{\frac{-Rt}{L}} \cdot \cos\theta}{1 - e^{\frac{-Rt}{L}}}\right)$

A typical current waveform may be as shown in Fig.4.7.

It can be seen that SCR 1 does not stop conduction even when the supply voltage has reversed. Thyristor 1 conducts till the current through it passes through zero. Then SCR 1' starts conducting. Forced commutation occurs when the current through SCR 1' is passing through its peak. The capacitor discharge through SCRs 1' and 2' turns off 1'. But the load current has not reversed, therefore 2' is also turned off and instead SCR 2 begins to conduct and returns the load inductive energy to the supply. When the current through load passes through zero, SCR 2' starts conducting as its gate is still positive and continues to conduct till the current through the load reverses and SCR 2 conducts again.

It is to be noted that SCR 1' or 2 do not start conducting just when the voltage reverses but go into conduction when the load current reverses. With a phase shifted sinusoidal gating signal a situation may arise (depending upon how much inductive the load is) that the SCRs 1' or 2' may not go into dunction because of the insufficient gate signal strength. Therefore, in an inductive load the use of a rectangular gating signal in quadrature with the supply input should be preferred or else an increase in the sinusoidal gating signal and the adjustment in phase shift may serve the purpose.

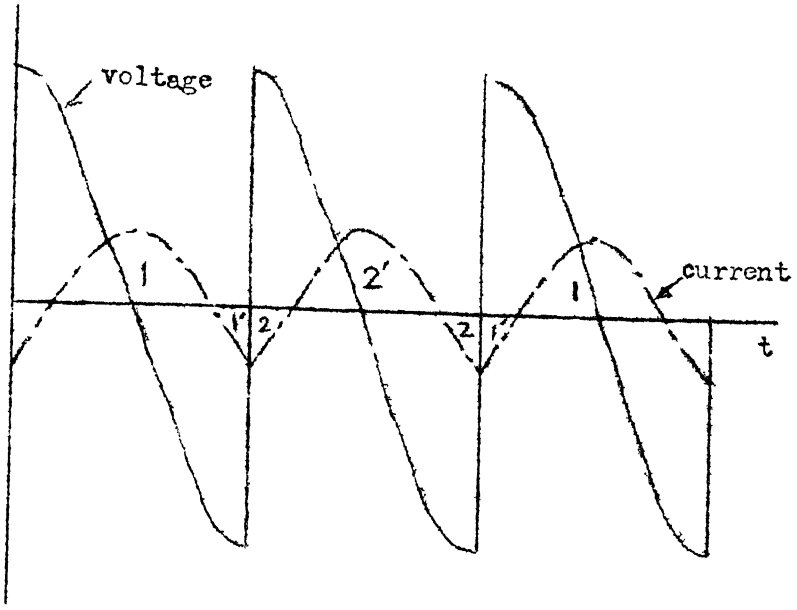


Fig. 4.7 Voltage and Current relation for an inductive load

Fig.4.9(a)

Fig. 4.9(b)

4 6 Analysis during the Commutating Interval :

The analysis has been carried out for resistive load only, for the presence of load inductance makes the analysis quite complex.

For this analysis the following assumptions have been made.

(1) The input remains constant at the value E_m during the the commutating interval and hence the expressions will apply only for that interval.

(2) The transformer is an ideal transformer with negligible magnetising current and negligible winding resistance and reactance.

(3) The commutating inductance has negligible resistance.

(4) The SCRs are ideal with zero forward resistance when 'on', infinite forward resistance when 'off', and infinite reverse resistance.

(5) The load contains resistance only.

When SCR 1' is conducting and the voltage is passing through its maxima, SCR 2' is to be switched 'on'. The capacitor is charged to a voltage 2 E_m at this instant.

Drawing the equivalent circuit (Fig.4.8a) and transforming the circuit to a convenient form as shown in Figs. 4.8(b) and 4.8(c). In the Fig.4.8(b), the circuit between nodes A and B can be reduced to a simpler

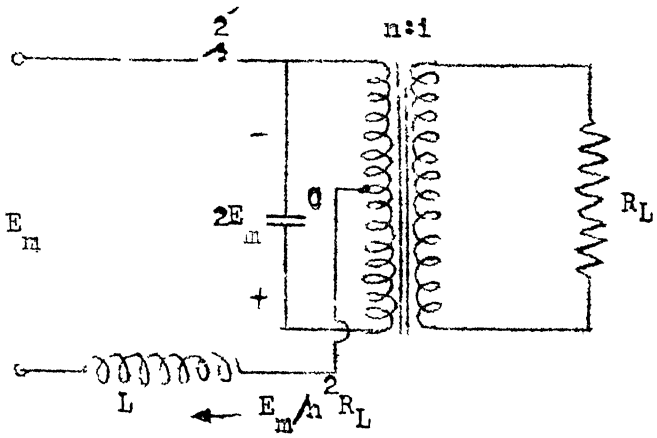
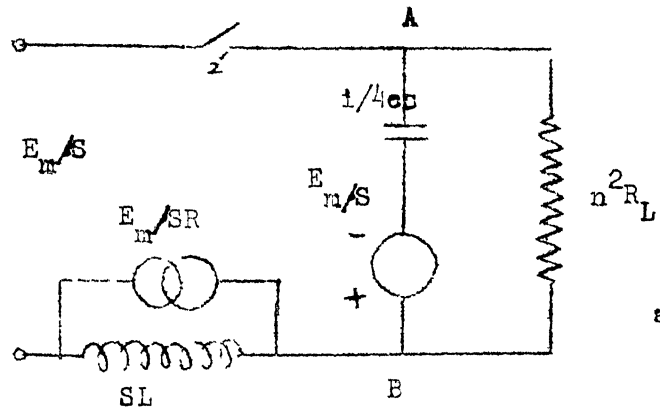


Fig. 4.8(a)



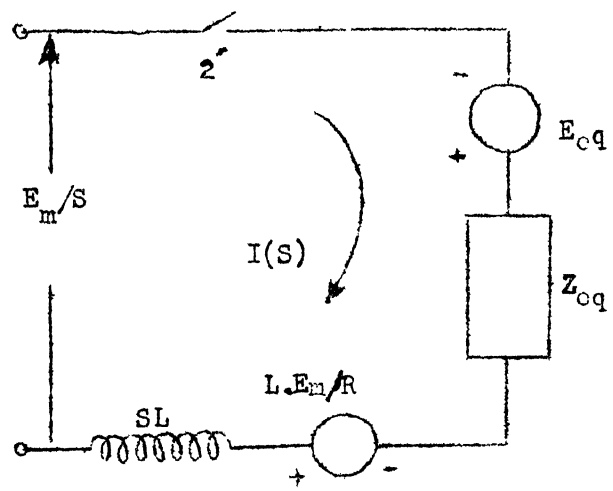
Define

$R' = n^2 R_L$

and

$4C = C'$

Fig. 4.8(b)



where

$E_{eq} = E_m \cdot R \cdot C'/1+SRC'$

$Z_{eq} = R/1+SCR$

Fig. 4.8 (c)

form by the application of Thevenin's theorem.

$$Z_{eq} = \frac{R/SC'}{R+1/SC'} = \frac{R}{1+SC'R}$$

where

$$R = n^2 R_L \quad \text{and} \quad C' = 4C$$

$$E_{eq} = \frac{E_m R/S}{R+1/SC'} = \frac{E_m RC'}{1+SRC'}$$

The voltage equivalent source which will replace the current source E_m/SR is $(E_m/SR)SL = E_m(L/R)$

Writing the loop equation

$$\frac{E_m}{S} + \frac{E_m L}{R} + \frac{E_m RC'}{1+SRC'} = I(S)\left(SL + \frac{R}{1+SC'R}\right)$$

$$\text{or} \quad I(S) = \frac{E_m}{R} \times \left[\frac{1+2SRC' + SL/R + S^2LC'}{S(SL/R + S^2LC' + 1)}\right]$$

Defining $RC' = T_c$ and $L/R = T_L$

$$I(S) = \frac{E_m}{R} \times \left[\frac{1+2T_cS + ST_L + S^2T_c \cdot T_L}{S(ST_L + S^2\ T_c \cdot T_L + 1)}\right]$$

Taking the inverse Laplace transform, the thyristor 2 current is

$$I(t) = \frac{E_m}{R}\left[1 + \frac{2T_c/T_L}{(T_c/T_L - 1)^{\frac{1}{4}}}\ e^{-t/2T_c}\ \text{Sin}\ \frac{1}{T_c}\left(\frac{T_c}{T_L} - \tfrac{1}{4}\right)^{\frac{1}{2}} t\right]$$

If $Q = \left(\frac{T_c}{T_L} - \frac{1}{4}\right)^{\frac{1}{2}}$, $Q^2 + \frac{1}{4} = \frac{T_c}{T_L}$

$$I(t) = \frac{E_m}{R}\left[1+\frac{2(Q^2+\frac{1}{4})}{Q}\, e^{-t/2T_c}\ \ \mathrm{Sin}\ \frac{Qt}{T_c}\right]$$

for $T_c/T_L < \frac{1}{4}$, Q is imaginary and the current increases exponentially.

The output voltage transform is

$$V_L(S) = I(S)\ (R/1 + SCR)$$

Simplifying and taking the inverse Laplace transform,

$$V_L(t) = E_m\left[1 - 2e^{-t/2T_c}\ \mathrm{Cos}\ \frac{Qt}{T_c} + \frac{1}{Q}\, e^{-t/2T_c}\ .\mathrm{Sin}\ \frac{Qt}{T_c}\right]$$

From the equation for the output voltage, it will be seen that the thyristor ceases to be reverse biased when the output voltage goes through zero The slope of the output voltage waveform at the instant of switching i.e., at $t = 0$ is

$$\left.\frac{dV_L}{dt}\right|_{t=0} = \frac{2E_m}{T_c} \text{ volts/sec}$$

Considering the slope constant until voltage passes through zero, zero will be passed at a time T

$$T = T_c/2$$

and if this time T is greater than the commutation time of the thyristor satisfactory commutation will take place.

$$\therefore \quad t_{off} < \frac{T_c}{2} \text{ sec.}$$

To be on the safe side the inequality $t_{off} < T_c/3$ will be used.

Figures 4 9(a) and 4 9(b) show the output voltage waveforms for two different values of T_c/T_L The one with more oscillations in the commutating interval is for higher ratio of T_c/T_L.

4.7 Harmonics in the Output .

Considering a general case of cosine waveform (Fig.4.1 between θ_1 and θ_2 and representing it by Fourier series

$$f(\theta) = a_0 + \sum_{n=1}^{\infty} \left(a_n \text{ Cos } n\theta + b_n \text{ Sin } n\theta\right)$$

In the present case

$$f(\theta) = \frac{E_m}{\pi} \left[\frac{4}{3} \text{ Sin } 2\theta + \frac{8}{15} \text{ Sin } 4\theta + \frac{15}{35} \text{ Sin } 6\theta + \frac{16}{63} \text{ Sin } 8\theta \right]$$

for $\theta_1 = 0$ and $\theta_2 = 180^\circ$ as shown in Appendix 4.3.

If the amplitude of second harmonic ($4E_m/3$) is taken as 100%, then

% 4th harmonic or second harmonic with respect to double frequency = 40%.

% 6th harmonic or 3rd harmonic with respect to double frequency = 25.7% and so on

The percentages of various harmonics present in the output have been plotted in Fig.4.11.

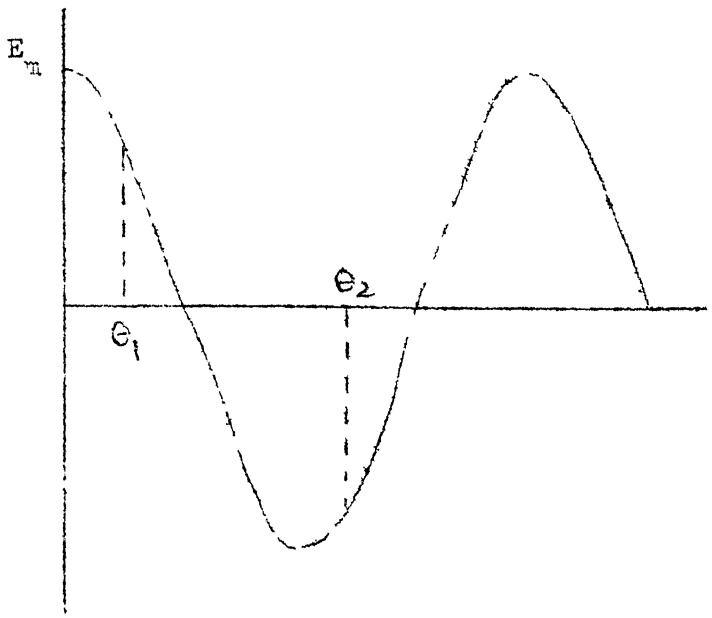


Fig. 4.10 General Cosine Section

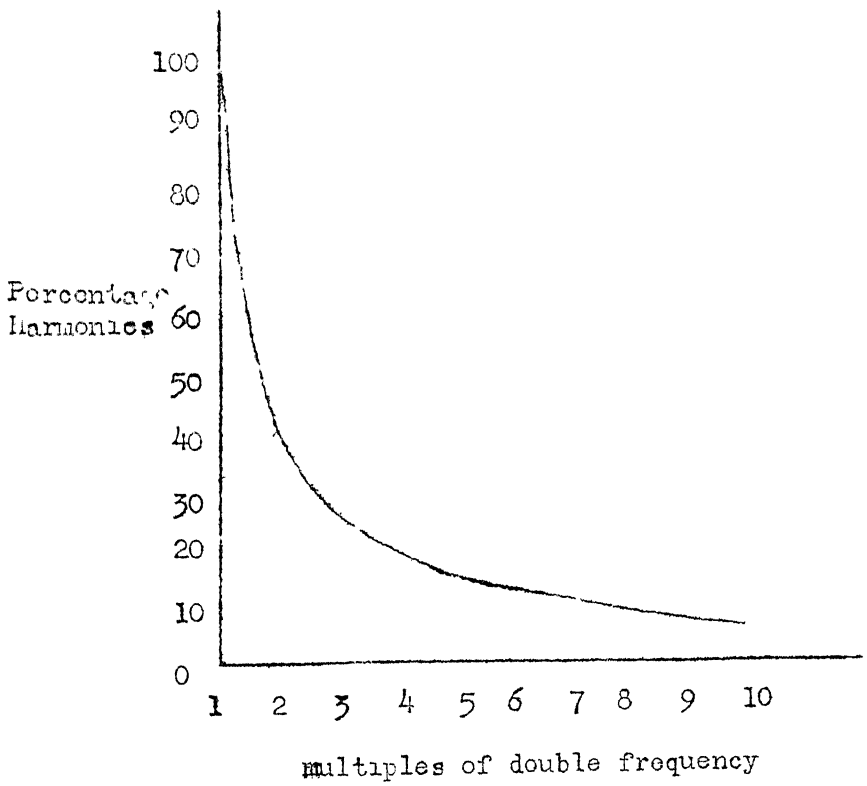


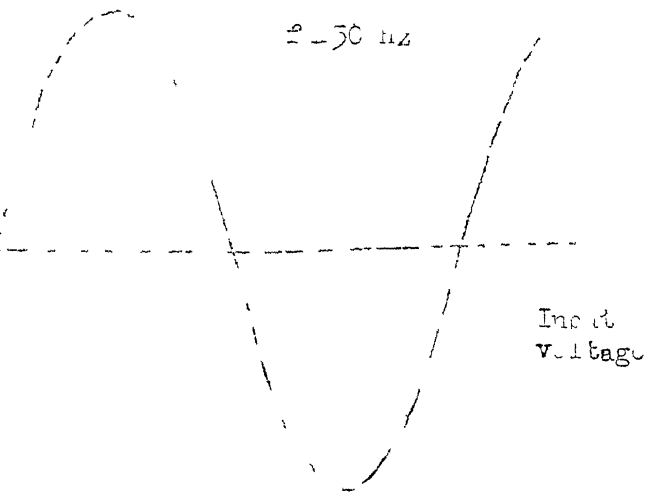
Fig.4.11 Harmonic Plot

4.8 General Frequency Multiplier

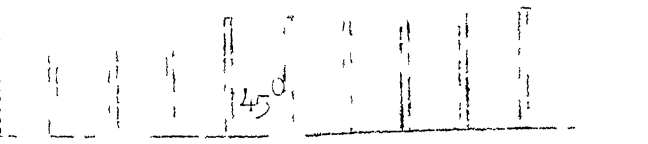
The circuit discussed in Section 4.5 can also be used to produce higher frequency output. This can be done by suitably choosing the SCR firing interval. For frequency tripling the firing interval is 60° and for frequency multiplication by a factor four, this interval is 45°. For an odd frequency multiplication factor, there will be a net primary D.C ampere turns but for an even frequency multiplication factor, the net D.C ampere turns are zero. This is clear from the output waveforms shown in Fig.4.12(c) and Fig.4.13(c). The outputs of these frequency multipliers are found to be highly distorted.

4.9 Conclusions :

The frequency doubler circuit has an improved efficiency and regulation when compared to the frequency doublers discussed in Chapter II. In this case the output power cannot be varied by controlling the firing instants of SCRs. The output voltage waveform of this frequency doubler has more distortion contents when compared to the distortion contents of the output voltage of the frequency doubler discussed in Chapter II. The chief merit of this circuit over the circuits discussed previously, is that it requires a single phase supply input. The same circuit can be used for the generation of higher frequency output, if a suitable gate firing scheme is used.



(a)



(b)

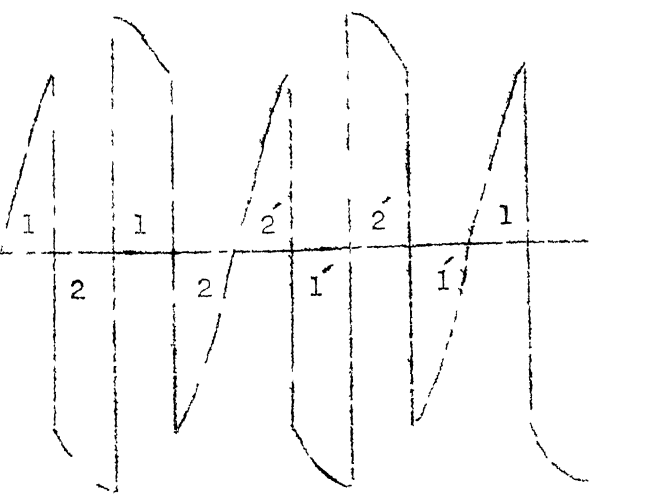
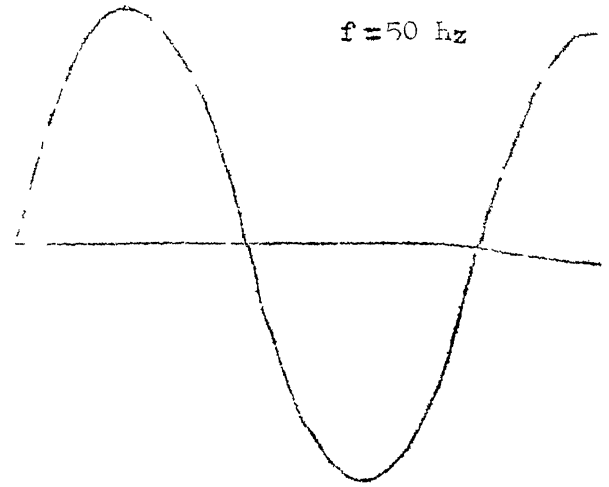
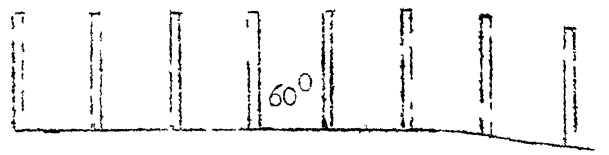


Fig.4.13(c) Frequency Quadrupler Output



(a)



(b)

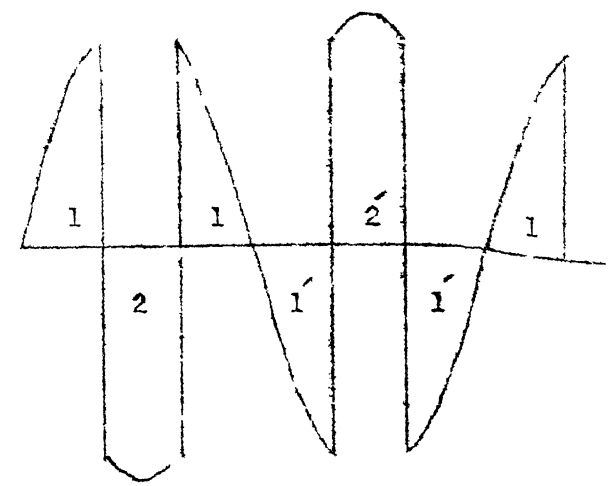


Fig.4.12(c) Frequency Trippler Output

CHAPTER V

CONCLUSIONS

In this thesis, various frequency doubler circuits are considered. These circuits are either using two phase supply input or a single phase supply input. It is pointed out that the circuits using two rectifier units and a subtraction unit, though give a reasonably sinusoidal output voltage waveform have very low efficiency and poor regulation. In the improved form of the frequency doubler circuit using two phase input, it is pointed out that the circuit efficiency is quite high but the distortion contents increase. It is shown that this circuit can also be applied for the generation of higher even harmonics.

In the end, a frequency doubler circuit with a single phase input is given. It is found that the circuit is quite efficient but gives out a much distorted output. This scheme has also been shown to be applicable for the generation of higher harmonics but distortion contents increase further.

Thus it is found that the efficiency of the frequency doubler circuits can be improved only at the cost of a good output voltage waveform.

It may be possible to extend the results to develop a general frequency multiplier with reasonably good output waveform and high efficiency by suitably modifying the circuits. This is considered as a problem for further research.

APPENDIX 2.1

Referring to Fig.2.5(a), the equations defining the rectified voltage waveform (1) are .

$$f(\theta) = 0 \qquad \text{for } 0 \leqslant \theta \leqslant \alpha$$

$$f(\theta) = E_m \operatorname{Sin} \theta \qquad \text{for } \pi \leqslant \theta \leqslant \pi$$

$$f(\theta) = 0 \qquad \text{for } \pi \leqslant \theta \leqslant \pi + \alpha$$

$$f(\theta) = - E_m \operatorname{Sin} \theta \qquad \text{for } \pi + \alpha < 0 < 2\pi$$

The Fourier coefficients a_o, a_n and b_n are given by the relations

$$a_o = \frac{E_m}{2\pi} \int_o^{2\pi} f(\theta).\, d\theta$$

$$a_n = \frac{E_m}{\pi} \int_o^{2\pi} f(\theta) \operatorname{Cosn}\theta . d\theta$$

and

$$b_n = \frac{E_m}{\pi} \int_o^{2\pi} f(\theta) \operatorname{Sin} n\theta . d\theta$$

Therefore,

$$a_o^{(1)} = \frac{E_m}{2\pi} \left(\int_\alpha^{\pi} \operatorname{Sin} \theta . d\theta - \int_{\pi+\alpha}^{2\pi} \operatorname{Sin} \theta . d\theta \right)$$

$$= \frac{E_m}{\pi} (1 + \operatorname{Cos} \alpha)$$

$$a_n^{(1)} = \frac{E_m}{\pi} \left(\int_\alpha^{\pi} \operatorname{Sin} \theta . \operatorname{Cos} n\theta . d\theta - \int_{\pi+\alpha}^{2\pi} \operatorname{Sin} \theta . \operatorname{Cos} n\theta . d\theta \right)$$

Using the trignometric relation

$$\text{Sin } C.\text{Cos } D = \frac{\text{Sin}(C+D) + \text{Sin}(C-D)}{2}$$

and integrating,

$$a_n^{(1)} = \frac{E_m}{2\pi}\left[\frac{\text{Cos}(n+1)\alpha}{n+1} - \frac{\text{Cos}(n-1)\alpha}{n-1} - \frac{\text{Cos}(n+1)\pi}{n+1} + \frac{\text{Cos}(n-1)\pi}{n-1} + \frac{\text{Cos}(n+1)2\pi}{n+1} - \frac{\text{Cos}(n+1)(\pi+\alpha)}{n+1} - \frac{\text{Cos}(n-1)2\pi}{n-1} + \frac{\text{Cos}(n-1)(\pi+\alpha)}{n-1}\right]$$

For odd values of n, $a_n^{(1)} = 0$.

For even values of n, after simplification, $a_n^{(1)}$ reduces to

$$a_n^{(1)} = \frac{E_m}{\pi}\left[\frac{1}{n+1} - \frac{1}{n-1} + \frac{\text{Cos}(n+1)\alpha}{n+1} - \frac{\text{Cos}(n-1)\alpha}{n-1}\right]$$

$$b_n^{(1)} = \frac{E_m}{\pi}\left(\int_{\alpha}^{\pi} \text{Sin } \theta \,.\, \text{Sin } n\theta.d\theta - \int_{\pi+\alpha}^{2\pi} \text{Sin } \theta \,.\, \text{Sin } n\theta.d\theta\right)$$

Using the relation

$$\text{Sin } C \,.\, \text{Sin } D = \frac{\text{Cos}(C-D) - \text{Cos}(C+D)}{2}$$

and integrating

$$b_n^{(1)} = \frac{E_m}{2\pi}\left[\frac{\text{Sin}(n-1)\pi}{n-1} - \frac{\text{Sin}(n-1)\alpha}{n-1} - \frac{\text{Sin}(n+1)\pi}{n+1} + \frac{\text{Sin}(n+1)\alpha}{n+1} - \frac{\text{Sin}(n-1)2\pi}{n-1} - \frac{\text{Sin}(n-1)(\pi+\alpha)}{n-1} - \frac{\text{Sin}(n+1)2\pi}{n+1} + \frac{\text{Sin}(n+1)(\pi+\alpha)}{n+1}\right]$$

For odd values of n, $b_n^{(1)} = 0$.

For even values of n, $b_n^{(1)}$ reduces to

$$b_n^{(1)} = \frac{E_m}{\pi}\left[\frac{\mathrm{Sin}(n+1)\alpha}{n+1} - \frac{\mathrm{Sin}(n-1)\alpha}{n-1}\right]$$

For the rectified voltage waveform (11), the defining equations are :

$$f(\theta) = 0 \qquad \text{for } -\frac{\pi}{2} \leqslant \theta \leqslant -\frac{\pi}{2} + \alpha$$

$$f(\theta) = E_m \cos\theta \qquad \text{for } -\frac{\pi}{2} + \alpha \leqslant \theta \leqslant \frac{\pi}{2}$$

$$f(\theta) = 0 \qquad \text{for } \frac{\pi}{2} \leqslant \theta \leqslant \frac{\pi}{2} + \alpha$$

and $$f(\theta) = -E_m \cos\theta \qquad \text{for } \frac{\pi}{2} + \alpha \leqslant \theta \leqslant 2\pi$$

The Fourier coefficients have been found out in a similar way as above.

$$a_o^{(11)} = \frac{E_m}{\pi}(1 + \cos\alpha)$$

$$a_n^{(11)} = \frac{E_m}{\pi}\left[\frac{\mathrm{Sin}(n+1)\pi/2}{n+1} - \frac{\mathrm{Sin}(n+1)(-\pi/2 + \alpha)}{n+1} + \frac{\mathrm{Sin}(n-1)\pi/2}{n-1} - \frac{\mathrm{Sin}(n-1)(-\pi/2 + \alpha)}{n-1}\right]$$

for even values of n only.

and

$$b_n^{(11)} = \frac{E_m}{\pi}\left[\frac{\cos(n+1)(-\pi/2 + \alpha)}{n+1} + \frac{\cos(n-1)(-\pi/2 + \alpha)}{n-1}\right]$$

for even values of n only.

APPENDIX 3.1

Referring to Fig.3.3 showing the output voltage waveform of the improved frequency doubler operating in mode I,

$$f(\theta) = 0 \qquad \text{for } 0 \leqslant \theta \leqslant \theta_1$$

$$f(\theta) = E_m \operatorname{Cos} \theta \qquad \text{for } \theta_1 \leqslant \theta \leqslant \pi/2$$

$$f(\theta) = 0 \qquad \text{for } \pi/2 \leqslant \theta \leqslant \theta_2$$

and $$f(\theta) = -E_m \operatorname{Sin} \theta \qquad \text{for } \theta_2 \leqslant \theta \leqslant \pi$$

The Fourier series representation of a function $f(\theta)$ is

$$f(\theta) = a_o + \sum_{n=1}^{\infty} a_n \operatorname{Cos} n\theta + b_n \operatorname{Sin} n\theta$$

where a_o, a_n and b_n in the present case are :

$$a_o = \frac{E_m}{2\pi} \left[\int_{\theta_1}^{\pi/2} \operatorname{Cos} \theta \, . \, d\theta - \int_{\theta_2}^{\pi} \operatorname{Sin} \theta . d\theta \right]$$

$$= \frac{E_m}{2\pi} (-\operatorname{Sin} \theta_1 - \operatorname{Cos} \theta_2)$$

For the case under consideration, θ_2 is equal to $\pi/2 + \theta_1$,

$$\therefore \quad a_o = 0.$$

$$a_n = \frac{E_m}{\pi} \left(\int_{\theta_1}^{\pi/2} \operatorname{Cos} \theta \, . \, \operatorname{Cos} n\theta . d\theta - \int_{\theta_2}^{\pi} \operatorname{Sin} \theta \, . \, \operatorname{Cos} n\theta . d\theta \right)$$

Using the relations

$$\operatorname{Cos} C \, . \, \operatorname{Cos} D = \frac{\operatorname{Cos}(C+D) + \operatorname{Cos}(C-D)}{2}$$

and $$\operatorname{Sin} C \, . \, \operatorname{Cos} D = \frac{\operatorname{Sin}(C+D) + \operatorname{Sin}(C-D)}{2}$$

and integrating

$$a_n = \frac{E_m}{2\pi}\left[\frac{\sin(1+n)\pi/2}{1+n} - \frac{\sin(1+n)\theta_1}{1+n} + \frac{\sin(1-n)\pi/2}{1-n} - \frac{\sin(1-n)\theta_1}{1-n} + \frac{\cos(1+n)\pi}{1+n} - \frac{\cos(1+n)\theta_2}{1+n} - \frac{\cos(n-1)\pi}{n-1} + \frac{\cos(n-1)\theta_2}{n-1}\right]$$

where $\theta_2 = \pi/2 + \theta_1$,

and

$$b_n = \frac{E_m}{\pi}\left(\int_{\theta_1}^{\pi/2} \cos\theta \cdot \sin n\theta . d\theta - \int_{\theta_2}^{\pi} \sin\theta \cdot \sin n\theta . d\theta\right)$$

Using the relations

$$\cos C . \sin D = \frac{\sin(C+D) - \sin(C-D)}{2}$$

$$\sin C . \sin D = \frac{\cos(D-C) - \cos(C+D)}{2}$$

and integrating

$$b_n = \frac{E_m}{2\pi}\left[-\frac{\cos(n+1)\pi/2}{n+1} + \frac{\cos(n+1)\theta_1}{n+1} - \frac{\cos(n-1)\pi/2}{n-1} + \frac{\cos(n-1)\theta_1}{n-1} + \frac{\sin(n-1)\theta_2}{n-1} - \frac{\sin(n+1)\theta_2}{n+1}\right]$$

APPENDIX 4.1

Two arrangements, one for phase shift between zero to 90^0 and another for phase shift between zero to 180^0 are given.

a) Phase Shift $0^0 - 90^0$:

Fig.1 shows the arrangement used for the purpose. Assuming i_g to be negligible as compared to i,

$$V_g = V_1 - i(R_1 + R_2)$$

$$= V_1 - \frac{V_1}{R + 1/jwC} R \qquad \text{where } R = R_1 + R_2$$

$$V_g = V_1 \frac{1}{1 + jwCR}$$

$$= \frac{V_1 \angle -\tan^{-1} wCR}{\sqrt{1 + w^2C^2R^2}}$$

When wCR is very large, phase shift approaches 90^0 and when wCR is very small, phase shift approaches 0^0. This variation in phase shift is achieved by varying R.

b) Phase Shift $0^0 - 180^0$:

In Fig.2 is given the R-C circuit for getting this variable phase shift.

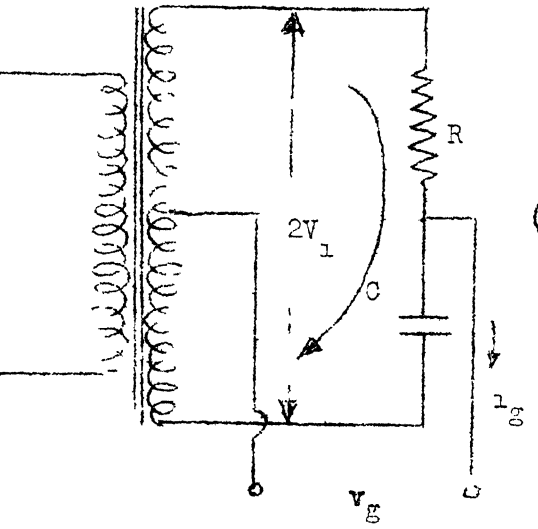


Fig. 2

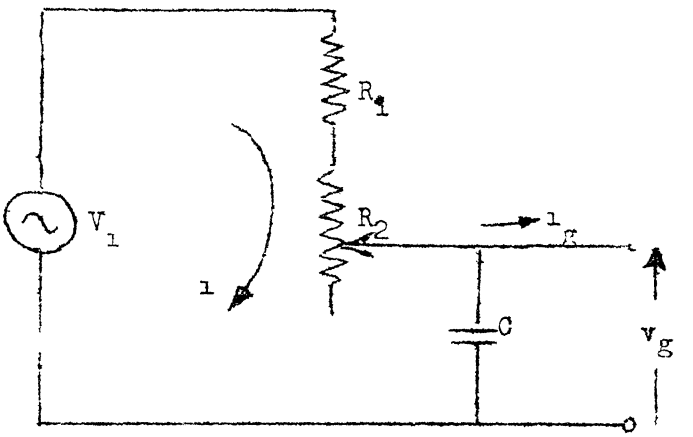
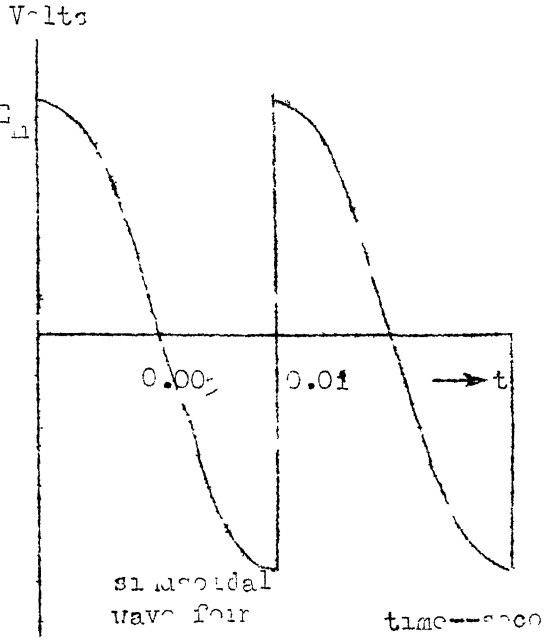


Fig 1

R-C Phase Shifting Circuits



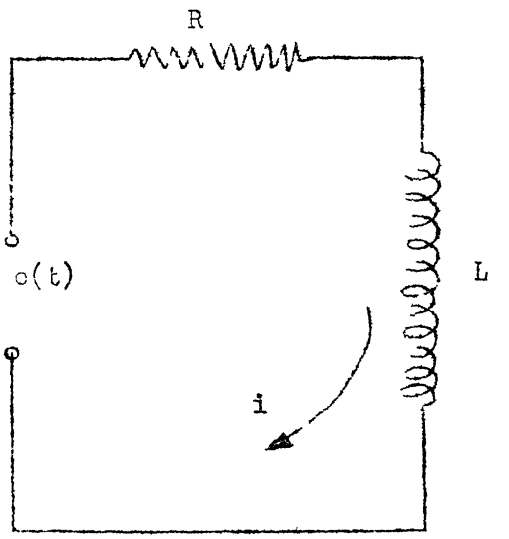


Fig. 3

Assuming that i_g is negligible when compared to i

$$V_g = V_1 - iR$$

$$= V_1 - \frac{2V_1}{R + 1/jwC} R$$

$$= V_1 \frac{1 - jwCR}{1 + jwCR} = V_1 \angle -2\tan^{-1} wCR .$$

When wCR is very large, the phase shift approaches 180°, and when wCR is very small, the phase shift approaches 0°. By varying R, the phase shift is varied between the two limits.

APPENDIX 4.2

In the case of inductive load the current lags the voltage. The nature of output voltage waveform does not undergo any substantial change due to the presence of load inductance, except during transients. But the load current waveform undergoes a major change.

Examining a R-L circuit to which the idealised output voltage of the frequency doubler has been applied (Fig.3). The steady state current expression is desired. The time interval of 0.01 second is the period of the repeating applied voltage, therefore if the current starts at a value i(0) at t = 0, it returns to same value at 0.01sec.

The 'response inside the cycle' is determined by the fact that at t = 0 the current has an i(0) value when the alternating voltage is applied to the circuit In this interval the circuit does not know that the voltage is going to change at t = 0.01 sec. The frequency of the sinewave, of which this voltage forms a part is 50 Hz.

The circuit equation for this interval is

$$E_m \cos 100\pi t = Ri + L \frac{di}{dt}$$

The current is composed of two components.

$$i = i_{ss} + i_{tr}$$

where i_{ss}, the steady state component is given by

$$i_{ss} = \frac{E_m}{Z} \text{ Cos } (wt - \theta)$$

where $\theta = \tan^{-1} \frac{wL}{R}$ and $Z = \sqrt{R^2 + w^2L^2}$

The transient component of the current $i_{tr} = Ae^{-Rt/L}$.

Therefore,

$$i = i_{ss} + i_{tr} = \frac{E_m}{Z} \text{ Cos } (wt - \theta) + Ae^{-Rt/L}$$

To find the constant A, imposing the condition that

$i = i(0)$ at $t = 0$

$$i(0) = \frac{E_m}{Z} \text{ Cos } \theta + A \quad \text{or} \quad A = i(0) - \frac{E_m}{Z} \text{ Cos } \theta$$

$$\therefore \quad i = \frac{E_m}{Z} \text{ Cos } (wt - \theta) + \left(i(0) - \frac{E_m}{Z} \text{ Cos } \theta \right) e^{-Rt/L}$$

Initial current $i(0)$ is found by substituting $i = i(0)$ at $t = 0.01$ and solving for $i(0)$

$$i(0) = \frac{\frac{E_m}{Z} \text{ Cos } (2\pi f \times 0.01 - \theta) - e^{-Rt/L} . \text{Cos } \theta}{1 - e^{-Rt/L}}$$

APPENDIX 4.3

Considering the general cosine section between θ_1 and θ_2 (Fig.4.10).

By Fourier analysis

$$f(\theta) = a_o + \sum_{n=1}^{\infty} a_n \operatorname{Cos} n\theta + b_n \operatorname{Sin} n\theta$$

where a_o, a_n and b_n are given by

$$a_o = \frac{E_m}{2\pi} \int_{\theta_1}^{\theta_2} f(\theta) d(\theta)$$

$$= \frac{E_m}{2\pi} \left(\int_{\theta_1}^{\theta_2} \operatorname{Cos} \theta . d\theta \right) = \frac{E_m}{2\pi} (\operatorname{Sin} \theta_2 - \operatorname{Sin} \theta_1)$$

If $\theta_1 = 0$ and $\theta_2 = \pi$ then $a_o = 0$

$$a_n = \frac{E_m}{\pi} \int_{\theta_1}^{\theta_2} f(\theta) \operatorname{Cos} n\theta . d\theta = \frac{E_m}{\pi} \int_{\theta_1}^{\theta_2} \operatorname{Cos} \theta \cdot \operatorname{Cos} n\theta . d\theta$$

$$= \frac{E_m}{\pi} \left(\int_{\theta_1}^{\theta_2} \frac{\operatorname{Cos} (1+n)\theta}{2} d\theta + \int_{\theta_1}^{\theta_2} \frac{\operatorname{Cos} (1-n)\theta}{2} d\theta \right)$$

$$= \frac{E_m}{2\pi} \left[\frac{\operatorname{Sin} (1+n)\theta_2 - \operatorname{Sin} (1+n)\theta_1}{1+n} + \frac{\operatorname{Sin} (1-n)\theta_1 - \operatorname{Sin} (1-n)\theta_2}{1-n} \right]$$

$a_n = 0$ for $\theta_1 = 0$ and $\theta_2 = \pi$ for all values of n

and $$b_n = \frac{E_m}{\pi} \int_{\theta_1}^{\theta_2} f(\theta) \operatorname{Sin} n\theta . d\theta = \frac{E_m}{\pi} \int_{\theta_1}^{\theta_2} \operatorname{Cos} \theta \cdot \operatorname{Sin} n\theta . d\theta$$

Integrating

$$b_n = \frac{E_m}{2\pi}\left[\frac{-\operatorname{Cos}(n+1)\theta_2 + \operatorname{Cos}(n+1)\theta_1}{n+1} + \frac{-\operatorname{Cos}(n-1)\theta_2 + \operatorname{Cos}(n-1)\theta_1}{n-1} \right]$$

when $\theta_1 = 0$ and $\theta_2 = \pi$

$$b_n = \frac{E_m}{2\pi}\left[\frac{1 - \operatorname{Cos}(n+1)\pi}{n+1} + \frac{1 - \operatorname{Cos}(n-1)\pi}{n-1} \right]$$

when n is odd, $b_n = 0$

and for even values of n

$$b_n = \frac{E_m}{\pi}\left(\frac{1}{n+1} + \frac{1}{n-1}\right).$$

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